140 x 2 0.6mm Pitch

FPGA I/O Bank 34
With 19 High-Speed
Differential Pairs

PHY

CAN0

BOARD POWER GOOD

WATCHDOG

JTAG

External Power Supply for FPGA Bank 13

PROGRAMMABLE
LOGIC
(PL)

Artix-7 FPGA
28K to 58K Logic Cells
17K to 53K LUTs
35K to 100K FF
240KB to 560KB RAM
80 to 220 DSP Slices

Dual ARM Cortex-A9 Core
@ 800MHz

Memory
Controller

PROCESSING SYSTEM (PS)

XILINX Zynq XC7Z010
or XC7Z020

Additional MIO Interfaces Through FPGA

SPI
MIO[6:1]

NAND
MIO[0, 14:2]

I2C0
MIO[47:46]

UART1
MIO[49:48]

USB
MIO[39:28]

ETH0
MIO[27:16]

SD0
MIO[45:40]

32 bits

DDR3
@ 533MHz

SPI0

Boot
NOR Flash

NAND
Flash

FPGA I/O Bank 13
With 12 High-Speed
Differential Pairs

Multiple
Voltage
Monitor

PSU

FPGA I/O Bank 35
with DDR Optimized
Interfacing/XADC
Signals

External Power Supply
for FPGA Bank 35

RTC
Sppm

Temp.
Sens.

UART

PHY

USB
OTG

PHY

ETH
10/100/
1000

SD CARD

140 x 2 0.6mm Pitch

140 x 2 0.6mm Pitch