PRESS Release

DAVE Embedded Systems

# AN-BELK-003: Interfacing DDR3 SDRAM to PL

Porcia, ITALY – September, 2015. As part of our standard service, DAVE Embedded Systems is proud to announce that we published on our wiki a NEW interesting Application Note around BELK titled “Interfacing DDR3 SDRAM to PL”.

CPU modules are characterized by direct addressing of hardware resources: NOR, NAND and RAM. BORA CPU module is not an exception.

However, in some scenarios it might be required to address also a secondary RAM bank dedicated to additional buffers or graphic memory.
To achieve that, users are supposed to design an IP in the programmable logic (PL) of Zynq and reserve a dedicated bank in
FPGA to guarantee exclusive access and to maximize bandwidth.
Moreover, this additional SDRAM bank is accessible via AXI bus and it is mapped in the processor's memory space, thus it can be accessed by the Zynq's PS as well.

BoraEVB can optionally be populated with a 16-bit 512MB SDRAM chip that is directly connected to PL.

This Application Note describes how to enable the support for this additional memory bank. An example Vivado design is released along with this application note, based on BELK 2.1.0

Read the full Application Note on the link below

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**Trademark:**

DAVE Embedded Systems is a well-established and constantly growing Italian company, focused on designing, manufacturing and selling of miniaturized embedded systems solutions. Since its foundation, back in 1998, DAVE Embedded Systems has developed its business, increasing its know-how and activities. Support and assistance provided to many Italian and foreign companies mainly concerns the design of microprocessor platforms, based on Linux, Windows or Android. DAVE Embedded Systems provides CPU modules solutions or System-On-Module (SoM) based on the latest technologies (e.g. Multi-Core ARM Cortex, PowerPC and X86) for the typical high-end markets such us medical and automotive.

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