AXEL ULite

ARM Cortex A7 MPCore
CPU Module

Lite Line

HARDWARE MANUAL

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1 Preface

1.1 About this manual

This Hardware Manual describes the **AXEL ULite** CPU module design and functions.

Precise specifications for the NXP i.MX6UL processor can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the **AXEL ULite** CPU module.

AXEL ULite CPU modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury.

DAVE Embedded Systems customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

DAVE Embedded Systems is guaranteed against defects in material and workmanship for the warranty period from the shipment date. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair or replace defective products. Within the warranty period, the repair of products is free of charge provided that warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the customer, unauthorized modification or misuse, operation outside of the product’s specifications or improper installation or maintenance.

DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty **AXEL ULite** module.

1.6 Technical Support

We are committed to making our product easy to use and will help customers use our CPU modules in their systems.

Technical support is delivered through email to our valued customers. Support requests can be sent to support-axel@dave.eu .

Software upgrades are available for download in the restricted access download area of DAVE Embedded Systems web site: http://www.dave.eu/reserved-area . An account is required to access this area and is provided to customers who purchase the development kit (please contact support-axel@dave.eu for account requests).

Please refer to our Web site at http://www.dave.eu/products/axel-lite for the latest product documentation, utilities, drivers, Product Change Notifications, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Developers Wiki	http://wiki.dave.eu/index.php/Main_Page

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
BTN	Button
EMAC	Ethernet Media Access Controller
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
PCB	Printed circuit board
PMIC	Power Management Integrated Circuit
PSU	Power supply unit
RTC	Real time clock
SOC	System-on-chip
SOM	System-on-module
WDT	Watchdog

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	*Date*	*Notes*
0.0.1	**June 2016**	**First draft (PRELIMINARY)**
0.9.0	**August 2016**	**First Release**
1.0.0	**September 2016**	**Release**
1.0.1	**December 2018**	**Minor fixes**
1.0.2	**August 2019**	**Minor fixes**

2 Introduction

AXEL ULite is the brand new solution made by DAVE Embedded Systems, based on the recent NXP/Freescale i.MX6UL Ultra Lite application processor. **AXEL ULite** defines a new limit in low power consumption with its ARM Cortex A7 architecture and enables customers to design a new concept of Embedded IoT devices.

Fig. 1: AXEL ULite

AXEL ULite offers great compromise between computing and power consumption, thanks to the ARM Cortex-A7 architecture. Additionally, the use of this processor enables extensive system-level differentiation of new applications in many industry fields, where power consumption, connectivity and extremely compact form factor (67,50 mm x around 25,40 mm) are key factors. The advanced security features and the three different CPU versions available (Base, General Purpose and Security) offer a wide scenario of applications. Smarter system designs are made possible, following the trends in functionalities and interfaces of the new, state-of-the-art embedded products.

2.1 Product Highlights

- ULTRA LOW POWER thanks to ARM Cortex A7 MPCore@528 MHz
- pin to pin compatibility with AXEL LITE SOM based on i.MX6
- i.MX6 software full compatibility
- High flexibility with up to 4 different scalable CPU versions (Base, General Purpose, Security)
- Advanced security thanks to TRNG, Crypto Engine, etc.
- Embedded IoT, connectivity version with "blind CPU"
- Boot from NOR for safe applications
- up to 2 x Ethernet 10/100 Mbps
- Single 3V3 Power Supply with very low power stand by or wide input 3.7-5.5V

2.2 Block Diagram

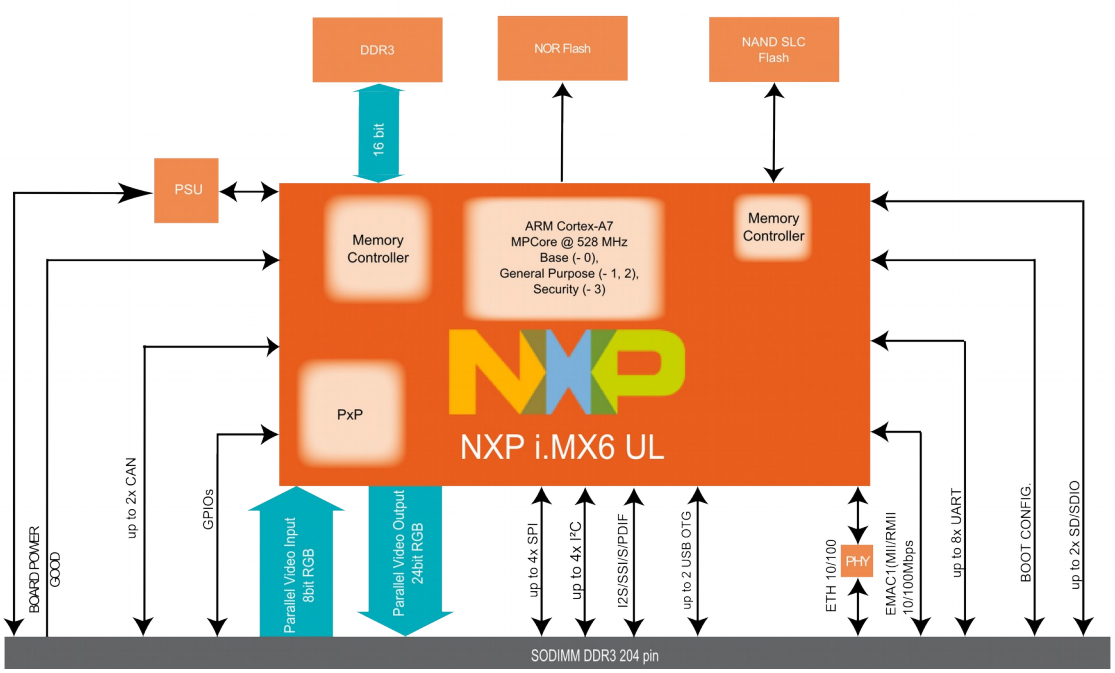

Fig. 2: AXEL ULite block diagram

2.3 Feature Summary

The following table summarizes the features available with **AXEL ULite**:

Feature	Specifications	Options
CPU	NXP/Freescale i.MX6 UL ARM Cortex A7 MPCore @ 528 MHz	
Cache	L1: 32 Kbyte instruction, 32 Kbyte data L2: Unified data/instruction, 128 K	
SDRAM	up to 512 DDR3 -LV, x16 data bus width	
NOR	SPI NOR 4 -32 MB on request	
NAND SLC	All sizes, on request	

Tab. 3: CPU, Memories, Buses

Feature	Specifications	Options
LAN	Ethernet 10/100 Mbps (PHY on board) additional MII/RMII interface	
Video Input	up to 1x CSI port 24 bit parallel	
Video Output	up to 1x RGB Parallel port 24 bit	
USB	up to 2x 2.0 OTG port (PHY on board)	
UARTs	up to 8x UART ports	
GPIO	GPIOs with interrupt capabilities up to 2x 8ch ADC (12bit) 8x8 Keypad	
CAN	up to 2x CAN	
PC CARD	up to 2x SD/MMC	
Audio	up to 3x I²S / SSI / S / PDIF	
Debug	JTAG IEEE 1149.1 Test Access Port	
Other	up to 4x I²C channels up to 4x SPI channels up to 8 PWM	

Tab. 4: Peripherals

Feature	Specifications	Options
Dimensions	67,50 mm x 25,40 mm	
Operating temperature range	Commercial (0°C / +70°C) Temperature Range Industrial (-40°C / +85°C) Temperature Range Extended (-40°C / +105°C) Temperature Range	
Weight	6.4 g	
Connectors	SODIMM 204 pin	

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of **AXEL ULite** module is composed by the following components:

- NXP i.MX6 UL core SoC application processor
- Power supply unit with 3V3 single rail or wide 3.7-5.5V input
- DDR memory bank
- NOR and NAND flash banks
- 204 pin SODIMM connector with interfaces signals. This chapter shortly describes the main **AXEL ULite** components.

3.1 NXP i.MX6UL application processor

The i.MX6UL processors feature NXP's advanced implementation of the ARM® Cortex®-A7 MPCore, which operates at speeds up to 528MHz. These SOCs include a deep encryption and security capability, a complex and flexible boot management and an integrated power management. As a result that the i.MX6UL devices are able to serve a wide range of applications including:

- Industrial gateways
- Instrument clusters, and portable medical devices.
- Dataloggers, remote control units
- Human-machine interfaces
- Safety blocks for IoT data manipulation and streaming

The i.MX6UL application processor is composed of the following major functional blocks:

- ARM Cortex-A7 MPCore CPU Processor, featuring:
- 128KB unified L2 cache
- NEON MPE co-processor
- External memories interconnect
- Connectivity peripherals, including
- 2xRMII - Ethernet 10/100 interfaces
- SD/SDIO/MMC
- Serial buses: USB, UART, I²C, SPI, CAN, …

- On G3 devices:
    - Security block, including
    - TRNG
    - Crypto Engine (AES with DPA, TDES/SHA/RSA)
    - Tamper Monitor
    - Secure Boot
    - SIMV2/EVMSIM X 2
    - OTF DRAM Encryption

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed by 16-bit width chip.

The following table reports the SDRAM specifications:

Dimension	Value
CPU connection	Multi-mode DDR controller (MMDC)
Size min	256 MB
Size max	512 GB
Width	16 bit
Speed	400 MHz

Tab. 6: DDR3 Specifications

3.2.1 Reliable Storage Strategy

Any embedded product requires to be reliable, robust and economic. This is the reason why DAVE Embedded Systems introduced the usage of a good combination of memories that works perfectly in their context and meet all embedded systems goals. NOR and NAND flash are the key components of this strategy.

[From Wiki]

NOR and NAND flash differ in two important ways:

- the connections of the individual memory cells are different
- the interface provided for reading and writing the memory is different (NOR allows random-access for reading, NAND allows only page access)

These two are linked by the design choices made in the development of NAND flash. A goal of NAND flash development was to reduce the chip area required to implement a given capacity of flash memory, and thereby to reduce cost per bit and increase maximum chip capacity so that flash memory could compete with magnetic storage devices like hard disks. [...]

Because of the series connection and removal of wordline contacts, a large grid of NAND flash memory cells will occupy perhaps only 60% of the area of equivalent NOR cells.

[..] NAND flash's designers realized that the area of a NAND chip, and thus the cost, could be further reduced by removing the external address and data bus circuitry. Instead, external devices could communicate with NAND flash via sequential-accessed command and data registers, which would internally retrieve and output the necessary data. This design choice made random-access of NAND flash memory impossible, but the goal of NAND flash was to replace mechanical hard disks, not to replace ROMs.

Attribute	NAND	NOR
Main Application	File Storage	Code execution
Storage capacity	High	Low
Cost per bit	Better	
Active Power	Better	
Stability Power		Better
Write Speed	Good	

Attribute	NAND	NOR
Read Speed		Good

Tab. 7: comparison

3.2.1.1 Write endurance

The write endurance of SLC floating-gate NOR flash is typically equal to or greater than that of NAND flash, while MLC NOR and NAND flash have similar endurance capabilities. Examples of endurance cycle ratings listed in datasheets for NAND and NOR flash are provided.

Type of flash memory	Endurance rating (Erases per block)	Example(s) of flash memory
SLC NAND	100,000	Samsung OneNAND KFW4G16Q2M
MLC NAND	5,000 to 10,000 for medium-capacity applications; 1,000 to 3,000 for high-capacity applications	Samsung K9G8G08U0M (Example for medium-capacity applications)
TLC NAND	1,000	Samsung 840
SLC (floating-gate) NOR	100,000 to 1,000,000	Numonyx M58BW (Endurance rating of 100,000 erases per block); Spansion S29CD016J (Endurance rating of 1,000,000 erases per block)
MLC (floating-gate) NOR	100,000	Numonyx J3 flash

Tab. 8: comparison

However, by applying certain algorithms and design paradigms such as wear leveling and memory over-provisioning, the endurance of a storage system can be tuned to serve specific requirements.[1]

1 https://en.wikipedia.org/wiki/Flash_memory#Distinction_between_NOR_and_NAND_flash

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This device is connected to the eCSPI channel 1. Specific models of the **AXEL ULite** SOM provide the SPI NOR as boot memory.

The following table reports the NOR flash specifications:

Dimension	Value
CPU connection	ECSPI1
Size min	4 MB
Size max	32 MB
Chip select	ECSPI1_SS0
Bootable	Yes

Tab. 9: NOR flash specifications

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash connected to the CPU's Raw NAND flash controller. Optionally, it can act as boot peripheral.

The following table reports the NAND flash specifications:

Dimension	Value
CPU connection	Raw NAND flash controller
Page Size	512 byte, 2 kbyte or 4 kbyte
Size min	128 MB
Size max	1 GB
Width	8 bit
Chip select	NANDF_CS0
Interface	asynchronous
technology	SLC
Bootable	Yes

Tab. 10: NAND flash specifications

3.5 Memory map

For detailed information, please refer to chapter 2 “Memory Maps” of the i.MX Applications Processor Reference Manual.

3.6 Power supply unit

AXEL ULite, as the other LITE Line CPU modules, embeds all the elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 7.1 Power Supply Unit (PSU) and recommended power-up sequence.

3.7 Power consumption

This section will be completed in a future version of this manual.

3.8 CPU module connectors

All interface signals **AXEL ULite** provides are routed through SODIMM DDR3 204 pin (named J2). The dedicated carrier board must mount the mating connector and connect the desired peripheral interfaces according to **AXEL ULite** pinout specifications.

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 5 (Pinout table) and 6 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the **AXEL ULite** SOM.

Mechanical drawings are available in DXF format on request.

4.1 Board Layout

The following figures shows the physical dimensions of the **AXEL ULite** module.

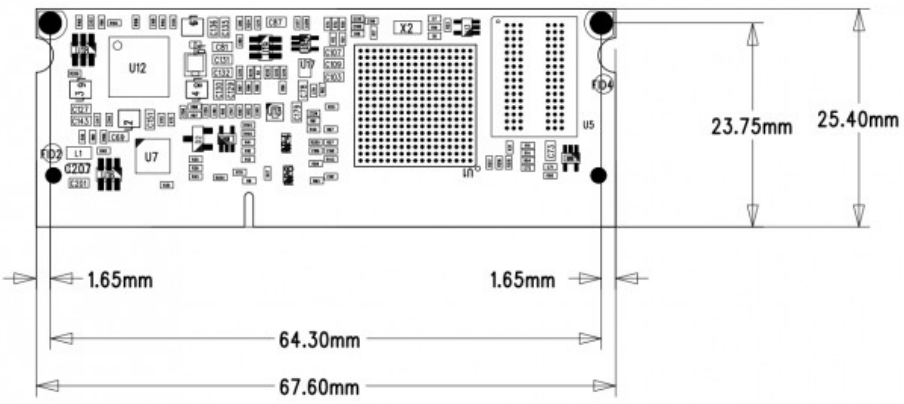

Fig. 3: Board layout - top view

4.2 Connectors

The following figure shows the **AXEL ULite** connectors layout:

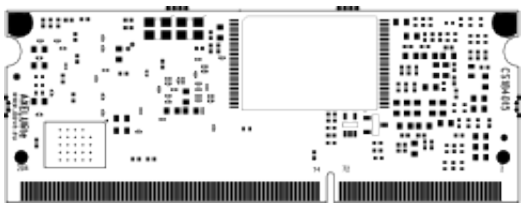

Fig. 4: Board bottom - top view

The following table reports connectors specifications:

Part number	Standard SO-DIMM 204-pin (DDR3)
Mating connectors	DDR3 SO-DIMM SOCKET Part number : TE Connectivity 2013289-1

4.3 Mechanical data table

All dimensions on the following table are in millimeters.

Dimension	Value
Width	67.60 mm
Depth	25.40 mm
Max components' height – top side	1.35 mm
Max components' height – bottom side	1.2 mm
PCB height	1.086 +-10
Weight	6.4 g

Tab. 11: mechanical data table

5 Pinout table

This chapter contains the pinout description of the **AXEL ULite** module, grouped in two tables (odd and even pins) that report the pin mapping of the 204-pin SO-DIMM **AXEL ULite** connector.

Each row in the pinout tables contains the following information:

Pin	Reference to the connector pin
Pin name	pin (signal) name on the AXEL ULite connectors
Internal Connections	connections to the AXEL ULite components CPU.<x> : pin connected to CPU pad named <x> PMIC.<x> : pin connected to the Power Manager IC LAN.<x> : pin connected to the LAN PHY
Ball/pin #	Component ball/pin number connected to signal

Tab. 12: pinout table

5.1 Carrier board mating connector J2

J2 odd pins (1 to 203)				
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Notes**
J2.1	DGND	DGND		
J2.3	3.3VIN	INPUT VOLTAGE		
J2.5	3.3VIN	INPUT VOLTAGE		
J2.7	3.3VIN	INPUT VOLTAGE		
J2.9	3.3VIN	INPUT VOLTAGE		
J2.11	DGND	DGND		
J2.13	ETH_LED1	LAN.LED0/PME_N1	23	
J2.15	VDDA_ADC_3P3			Reference voltage for SOC's ADC. Nominal value is 3.0V
J2.17	DGND	DGND		
J2.19	ETH_TX_P	LAN.TXP	6	

J2.21	ETH_TX_M	LAN.TXM	5	
J2.23	ETH_RX_P	LAN.RXP	4	
J2.25	ETH_RX_M	LAN.RXM	3	
J2.27	SNVS_TAMPER0	CPU.SNVS_TAMPER0	R10	
J2.29	SNVS_TAMPER1	CPU.SNVS_TAMPER1	R9	
J2.31	SNVS_TAMPER2	CPU.SNVS_TAMPER2	P11	Internally connected to ethernet PHY INT signal
J2.33	SNVS_TAMPER3	CPU.SNVS_TAMPER3	P10	
J2.35	DGND	DGND		
J2.37	SNVS_TAMPER4	CPU.SNVS_TAMPER4	P9	
J2.39	CSI_HSYNC	CPU.CSI_HSYNC	F3	
J2.41	SNVS_TAMPER5	CPU.SNVS_TAMPER5	N8	
J2.43	SNVS_TAMPER6	CPU.SNVS_TAMPER6	N11	
J2.45	SNVS_TAMPER7	CPU.SNVS_TAMPER7	N10	
J2.47	SNVS_TAMPER8	CPU.SNVS_TAMPER8	N9	
J2.49	SNVS_TAMPER9	CPU.SNVS_TAMPER9	R6	
J2.51	CSI_PIXCLK	CPU.CSI_PIXCLK	E5	
J2.53	CSI_MCLK	CPU.CSI_MCLK	F5	
J2.55	PMIC_VSNVS	PMIC.VSNVS	34	
J2.57	DGND	DGND		
J2.59	VPWR	PMIC.VPWR	31	
J2.61	VLDO2	PMIC.VLDO2	15	
J2.63	VLDO2	PMIC.VLDO2	15	
J2.65	UART5_RX_DATA	CPU.UART5_RX_DATA	G13	
J2.67	UART5_TX_DATA	CPU.UART5_TX_DATA	F17	
J2.69	VLDO3	PMIC.VLDO3	20	
J2.71	VLDO3	PMIC.VLDO3	20	
J2.73	DGND	DGND		
J2.75	SD1_DATA0	CPU.SD1_DATA0	B3	
J2.77	SD1_DATA1	CPU.SD1_DATA1	B2	
J2.79	SD1_DATA2	CPU.SD1_DATA2	B1	
J2.81	SD1_DATA3	CPU.SD1_DATA3	A2	
J2.83	SD1_CMD	CPU.SD1_CMD	C2	
J2.85	SD1_CLK	CPU.SD1_CLK	C1	
J2.87	DGND	DGND		
J2.89	GPIO1_IO04	CPU.GPIO_IO04	M16	
J2.91	GPIO1_IO05	CPU.GPIO_IO05	M17	
J2.93	ENET2_RX_DATA1	CPU.ENET2_RX_DATA1	C16	
J2.95	ENET2_RX_DATA0	CPU.ENET2_RX_DATA0	C17	
J2.97	ENET2_TX_DATA0	CPU.ENET2_TX_DATA0	A15	

J2.99	ENET2_RX_EN	CPU.ENET2_RX_EN	B17	
J2.101	ENET2_TX_CLK	CPU.ENET2_TX_CLK	D17	
J2.103	ENET2_RX_ER	CPU.ENET2_RX_ER	D16	
J2.105	ENET2_TX_EN	CPU.ENET2_TX_EN	B15	
J2.107	ENET2_TX_DATA1	CPU.ENET2_TX_DATA1	A16	
J2.109	DGND	DGND		
J2.111	N.C.			Not connected. Leave this pin floating.
J2.113	N.C.			Not connected. Leave this pin floating.
J2.115	N.C.			Not connected. Leave this pin floating.
J2.117	N.C.			Not connected. Leave this pin floating.
J2.119	N.C.			Not connected. Leave this pin floating.
J2.121	N.C.			Not connected. Leave this pin floating.
J2.123	N.C.			Not connected. Leave this pin floating.
J2.125	N.C.			Not connected. Leave this pin floating.
J2.127	GPIO1_IO06	CPU.GPIO_IO06	K17	Internally connected to ethernet PHY (MDIO)
J2.129	GPIO1_IO07	CPU.GPIO_IO07	L16	Internally connected to ethernet PHY (MDC)
J2.131	DGND	DGND		
J2.133	CSI_DATA04	CPU.CSI_DATA04	D4	Internally connected to NOR SPI flash
J2.135	CSI_DATA05	CPU.CSI_DATA05	D3	Internally connected to NOR SPI flash
J2.137	CSI_DATA07	CPU.CSI_DATA06	D2	Internally connected to NOR SPI flash
J2.139	CSI_DATA06	CPU.CSI_DATA07	D1	Internally connected to NOR SPI flash
J2.141	NVCC_ENET	CPU.NVCC_ENET	F13	
J2.143	CPU_VDD_SNVS_IN	CPU.VDD_SNVS_IN	P12	This is SoC's power rail of the SNVS domain. Please note that some SOC's GPIOs belong to this power domain
J2.145	N.C.			Not connected. Leave this pin floating.
J2.147	N.C.			Not connected. Leave this pin floating.

J2.149	UART4_RX_DATA	CPU.UART4_RX_DATA	G16	Internally connected to PMIC (used as I2C1 SDA)
J2.151	UART4_TX_DATA	CPU.UART4_TX_DATA	G17	Internally connected to PMIC (used as I2C1 SCL)
J2.153	DGND	DGND		
J2.155	N.C.			Not connected. Leave this pin floating.
J2.157	N.C.			Not connected. Leave this pin floating.
J2.159	N.C.			Not connected. Leave this pin floating.
J2.161	N.C.			Not connected. Leave this pin floating.
J2.163	N.C.			Not connected. Leave this pin floating.
J2.165	N.C.			Not connected. Leave this pin floating.
J2.167	N.C.			Not connected. Leave this pin floating.
J2.169	N.C.			Not connected. Leave this pin floating.
J2.171	N.C.			Not connected. Leave this pin floating.
J2.173	N.C.			Not connected. Leave this pin floating.
J2.175	DGND	DGND		
J2.177	UART1_nRTS	CPU.UART1_nRTS	J14	
J2.179	UART2_nRTS	CPU.UART2_nRTS	H14	
J2.181	UART2_nCTS	CPU.UART2_nCTS	J15	
J2.183	GPIO1_IO02	CPU.GPIO_IO02	L14	
J2.185	N.C.			Not connected. Leave this pin floating.
J2.187	UART1_TX_DATA	CPU.UART1_TX_DATA	K14	
J2.189	UART1_RX_DATA	CPU.UART1_RX_DATA	K16	
J2.191	UART3_TX_DATA	CPU.UART3_TX_DATA	H17	
J2.193	UART3_RX_DATA	CPU.UART3_RX_DATA	H16	
J2.195	UART3_nCTS	CPU.UART3_nCTS	H15	
J2.197	UART3_nRTS	CPU.UART3_nRTS	G14	
J2.199	GPIO1_IO03	CPU.GPIO_IO03	L17	
J2.201	UART1_CTS_B	CPU.UART1_nCTS	K15	
J2.203	DGND	DGND		

Tab. 13: J2 odd pins (1 to 203)

J2 even pins (2 to 204)				
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Notes**
J2.2	DGND	DGND		
J2.4	3.3VIN	INPUT VOLTAGE		
J2.6	3.3VIN	INPUT VOLTAGE		
J2.8	3.3VIN	INPUT VOLTAGE		
J2.10	3.3VIN	INPUT VOLTAGE		
J2.12	DGND	DGND		
J2.14	PMIC_LICELL	PMIC.LICELL	36	
J2.16	CPU_ONOFF	CPU.CPU_ONOFF	R8	
J2.18	SOM_PGOOD			Internally connected to 150K pull-down
J2.20	BOOT_MODE0	CPU.BOOT_MODE0	T10	Reset_scheme_(AXEL ULite)
J2.22	CPU_PORn	CPU.PORn	P8	
J2.24	PMIC_PWRON	PMIC.PWRON	48	
J2.26	BOOT_MODE1	CPU.BOOT_MODE1	U10	Reset_scheme_(AXEL ULite)
J2.28	GPIO1_IO08	CPU.GPIO_IO08	N17	Reset_scheme_(AXEL ULite)#Handling_CPU-initiated_software_reset
J2.30	DGND	DGND		
J2.32	CPU_PMIC_STBY_REQ	CPU.CCM_PMIC_STBY_REQ	U9	
J2.34	JTAG_TMS	CPU.JTAG_TMS	P14	
J2.36	PMIC_LDOG	PMIC.LDOG	30	
J2.38	GPIO1_IO00	CPU.GPIO_IO00	K13	
J2.40	PMIC_SNVS_OUT	PMIC.SNVS_OUT	34	This is normally left open.
J2.42	UART2_TX_DATA	CPU.UART2_TX_DATA	J17	
J2.44	UART2_RX_DATA	CPU.UART2_RX_DATA	J16	
J2.46	CSI_VSYNC	CPU.CSI_VSYNC	F2	
J2.48	GPIO1_IO01	CPU.GPIO_IO01	L15	
J2.50	PMIC_5V	PMIC.BST	37	PMIC 5V output (boost regulator)
J2.52	PMIC_5V	PMIC.BST	37	PMIC 5V output (boost regulator)
J2.54	N.C.			Not connected. Leave this pin floating.

J2.56	DGND	DGND		
J2.58	GPIO1_IO09	CPU.GPIO_IO09	M15	
J2.60	N.C.			Not connected. Leave this pin floating.
J2.62	JTAG_VREF	CPU.JTAG_VREF		Internally connected to 240 ohm pull-up to 3V3
J2.64	JTAG_MOD	CPU.JTAG_MOD	P15	Internally connected to 10K pull-down
J2.66	JTAG_TDI	CPU.JTAG_TDI	N16	
J2.68	JTAG_nTRST	CPU.JTAG_nTRST	N14	
J2.70	JTAG_TDO	CPU.JTAG_TDO	N15	
J2.72	JTAG_TCK	CPU.JTAG_TCK	M14	
J2.74	CSI_DATA00	CPU.CSI_DATA00	E4	
J2.76	CSI_DATA02	CPU.CSI_DATA02	E2	
J2.78	CSI_DATA03	CPU.CSI_DATA03	E1	
J2.80	CSI_DATA01	CPU.CSI_DATA01	E3	
J2.82	DGND	DGND		
J2.84	NAND_READY#	CPU.NAND_READY	A3	Internally connected to NAND flash
J2.86	NAND_CLE	CPU.NAND_CLE	A4	Internally connected to NAND flash
J2.88	NAND_ALE	CPU.NAND_ALE	B4	Internally connected to NAND flash
J2.90	NAND_RE#	CPU.NAND_RE	D8	Internally connected to NAND flash
J2.92	NAND_WE#	CPU.NAND_WE	C8	Internally connected to NAND flash
J2.94	NAND_WP#	CPU.NAND_WP	D5	Internally connected to NAND flash
J2.96	NAND_CS0#	CPU.NAND_CE0	C5	Internally connected to NAND flash
J2.98	NAND_CS1#	CPU.NAND_CE1	B5	Internally connected to NAND flash
J2.100	DGND	DGND		
J2.102	NAND_DQS	CPU.NAND_DQS	E6	Internally connected to NAND flash
J2.104	NAND_DATA00	CPU.NAND_DATA00	D7	Internally connected to NAND flash
J2.106	NAND_DATA01	CPU.NAND_DATA01	B7	Internally connected to NAND flash
J2.108	NAND_DATA02	CPU.NAND_DATA02	A7	Internally connected to NAND flash
J2.110	NAND_DATA03	CPU.NAND_DATA03	D6	Internally connected to

				NAND flash
J2.112	NAND_DATA04	CPU.NAND_DATA04	C6	Internally connected to NAND flash
J2.114	NAND_DATA05	CPU.NAND_DATA05	B6	Internally connected to NAND flash
J2.116	NAND_DATA06	CPU.NAND_DATA06	A6	Internally connected to NAND flash
J2.118	NAND_DATA07	CPU.NAND_DATA07	A5	Internally connected to NAND flash
J2.120	MEM_Wpn	MEM_Wpn		
J2.122	DGND	DGND		
J2.124	LCD_DATA_EN	CPU.LCD_ENABLE	B8	
J2.126	LCD_RESET	CPU.LCD_RESET	E9	
J2.128	LCD_VSYNC	CPU.LCD_VSYNC	C9	
J2.130	LCD_HSYNC	CPU.LCD_HSYNC	D9	
J2.132	LCD_CLK	CPU.LCD_CLK	A8	
J2.134	LCD_DATA00	CPU.LCD_DATA00	B9	
J2.136	LCD_DATA01	CPU.LCD_DATA01	A9	
J2.138	LCD_DATA02	CPU.LCD_DATA02	E10	
J2.140	LCD_DATA03	CPU.LCD_DATA03	D10	
J2.142	LCD_DATA04	CPU.LCD_DATA04	C10	
J2.144	LCD_DATA05	CPU.LCD_DATA05	B10	
J2.146	DGND			
J2.148	LCD_DATA06	CPU.LCD_DATA06	A10	
J2.150	LCD_DATA07	CPU.LCD_DATA07	D11	
J2.152	LCD_DATA08	CPU.LCD_DATA08	B11	
J2.154	LCD_DATA09	CPU.LCD_DATA09	A11	
J2.156	LCD_DATA10	CPU.LCD_DATA10	E12	
J2.158	LCD_DATA11	CPU.LCD_DATA11	D12	
J2.160	LCD_DATA12	CPU.LCD_DATA12	C12	
J2.162	LCD_DATA13	CPU.LCD_DATA13	B12	
J2.164	DGND			
J2.166	LCD_DATA14	CPU.LCD_DATA14	A12	
J2.168	LCD_DATA15	CPU.LCD_DATA15	D13	
J2.170	LCD_DATA16	CPU.LCD_DATA16	C13	
J2.172	LCD_DATA17	CPU.LCD_DATA17	B13	
J2.174	LCD_DATA18	CPU.LCD_DATA18	A13	
J2.176	LCD_DATA19	CPU.LCD_DATA19	D14	
J2.178	LCD_DATA20	CPU.LCD_DATA20	C14	
J2.180	LCD_DATA21	CPU.LCD_DATA21	B14	

J2.182	LCD_DATA22	CPU.LCD_DATA22	A14	
J2.184	LCD_DATA23	CPU.LCD_DATA23	B16	
J2.186	USB_OTG2_VBUS	CPU.USB_OTG2_VBUS	U12	
J2.188	USB_OTG1_VBUS	CPU.USB_OTG1_VBUS	T12	
J2.190	DGND	DGND		
J2.192	N.C.			Not connected. Leave this pin floating.
J2.194	USB_OTG1_CHD#	CPU.USB_OTG1_CHD	U16	
J2.196	USB_OTG2_DN	CPU.USB_OTG2_DN	T13	
J2.198	USB_OTG2_DP	CPU.USB_OTG2_DP	U13	
J2.200	USB_OTG1_DP	CPU.USB_OTG1_DP	T15	
J2.202	USB_OTG1_DN	CPU.USB_OTG1_DN	U15	
J2.204	DGND	DGND		

Tab. 14: J2 even pins (2 to 204)

6 Peripheral interfaces

AXEL ULite modules implement a number of peripheral interfaces through the SO-DIMM connector. Some interfaces/signals are available only with/without certain configuration options of the **AXEL ULite** module.

The signals for each interface are described in the related tables. The following notes summarize the column headers for these tables:

- “Pin name” – The symbolic name of each signal
- “Conn. Pin” – The pin number on the module connectors
- “internal connections” – Signal description
- “Ball/pin#” – ball7pin# for the 14x14mm BGA package

In the following sections are described in detail the HW configuration of available peripherals. The i.MX6UL SOC is highly configurable and enable users to change the pin configuration.

- In section 6.1 are described the HW configurations of those peripherals that can not change position such us ethernet, USBs, etc.
- In section 6.2 are described the peripherals that can change position
  - Section 6.2.1: Full GPIO configuration. All configurable pins are set as GPIO
- In section 6.3 are described 3 different standard configuration DAVE Embedded Systems has already tested and validate, for those customers that have no particular requirements:
  - Section 6.3.1: HMI configuration. The configurable pins are set in order to design a standard HMI machine
  - Section 6.3.2: IoT gateway configuration. The configurable pins are set in order to design a standard IoT gateway.
  - Last but not least, for those customers that wants to define their own pin muxing, in section 6.3.3 is described how to access the necessary information and how DAVE Embedded Systems can support them along this activity.

6.1 Fixed HW peripherals

Fixed HW peripherals are the devices connected on dedicated pins and are not to multiplexing and can not be multiplexed for other functionalities

In the sections below you can find the different standard devices within their system configuration

6.1.1 Ethernet

On-board Ethernet PHY (Micrel KSZ8019RN) provides interface signals required to implement the 10/100 Mbps Ethernet port. The transceiver is connected to the triple speed Ethernet MAC (ENET module) through RMII interface.

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
ETH_LED1	J2.13	LAN.LED0/PME_N1	23
ETH_TX_P	J2.19	LAN.TXP	6
ETH_TX_M	J2.21	LAN.TXM	5
ETH_RX_P	J2.23	LAN.RXP	4
ETH_RX_M	J2.25	LAN.RXM	3

Tab. 15: Ethernet interface signals

6.1.2 USB

AXEL ULite provides two USB 2.0 On-The-Go (OTG) ports with integrated PHY. Please note that the OTG_ID (USB mode host or device identifier) and the other power related signal as OTG_PWR (power) and OTG_OC (overcurrent) are multiplexed as alternate functions on different balls/connector pins.

6.1.2.1 USB OTG 1

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
USB_OTG1_VBUS	J2.188	CPU.USB_OTG1_VBUS	T12
USB_OTG1_CHD#	J2.194	CPU.USB_OTG1_CHD	U16
USB_OTG1_DP	J2.200	CPU.USB_OTG1_DP	U15
USB_OTG1_DN	J2.202	CPU.USB_OTG1_DN	T15

Tab. 16: USB1 interface signals

6.1.2.2 USB OTG 2

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
USB_OTG2_VBUS	J2.186	CPU.USB_OTG2_VBUS	U12
USB_OTG2_DN	J2.196	CPU.USB_OTG2_DN	T13
USB_OTG2_DP	J2.198	CPU.USB_OTG2_DP	U13

Tab. 17: USB2 interface signals

6.1.3 MMC/SD/SDIO

The processor provides 2 MMC/SD/SDIO ports through the Ultra Secured Digital Host Controller (USDHC), compliant with MMC V4.41, Secure Digital Memory Card Specification V3.00 and Secure Digital Input Output (SDIO) V3.00 specifications. The controller supports 1-bit / 4-bit SD and SDIO modes, 1-bit /4-bit / 8-bit MMC modes. High capacity SD cards (SDHC) are supported.

6.1.3.1 MMC/SD/SDIO1

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
SD1_CMD	J2.83	CPU.SD1_CMD	C2
SD1_CLK	J2.85	CPU.SD1_CLK	C1
SD1_DATA0	J2.75	CPU.SD1_DATA0	B3
SD1_DATA1	J2.77	CPU.SD1_DATA1	B2
SD1_DATA2	J2.79	CPU.SD1_DATA2	B1
SD1_DATA3	J2.81	CPU.SD1_DATA3	A2

Tab. 18: SD1 interface signals

The others SD1 pins – like SD1_CD, SD1_WP, etc. – are multiplexed on different balls/connector pins.

Even if this interface is the primary recovery boot interface (if the internal storage device is corrupted), its pins are multiplexed to many other interfaces (FLEXCAN1, FLEXCAN2, SAI1, USB power controls pins)

6.1.4 SPI

AXEL ULite provides up to four SPI ports connected to the i.MX6 integrated Enhanced Configurable SPI (ECSPI) controller, featuring:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Up to four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data

transfers

- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Configurable Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK)
- Direct Memory Access (DMA) support

6.1.5 ECSPI1

AXEL ULite on-board bootable SPI Flash is interfaced with the i.MX6UL through the eCSPI1 port on chip select 0. For further details, please refer to Section 3.3.

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
ECSPI1_SCLK	J2.133	CPU.CSI_DATA04	D4
ECSPI1_CS0	J2.135	CPU.CSI_DATA05	D3
ECSPI1_MOSI	J2.137	CPU.CSI_DATA06	D2
ECSPI1_MISO	J2.139	CPU.CSI_DATA07	D1

Tab. 19: ECSPI1 interface signals

6.1.6 NAND

AXEL ULite on-board bootable NAND Flash is interfaced with the i.MX6UL through the NAND controller port on chip select 0. For further details, please refer to Section 3.4.

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
NAND_READY#	J2.84	CPU.NAND_READY	A3
NAND_CLE	J2.86	CPU.NAND_CLE	A4
NAND_ALE	J2.88	CPU.NAND_ALE	B4
NAND_RE#	J2.90	CPU.NAND_RE#	D8
NAND_WE#	J2.92	CPU.NAND_WE#	C8
NAND_WP	J2.94	CPU.NAND_WP	D5
NAND_CS0#	J2.96	CPU.NAND_CE0	C5
NAND_CS1#	J2.98	CPU.NAND_CE1	B5
NAND_DQS	J2.102	CPU.AND_DQS	E6
NAND_DATA00	J2.104	CPU.NAND_DATA00	D7
NAND_DATA01	J2.106	CPU.NAND_DATA01	B7
NAND_DATA02	J2.108	CPU.NAND_DATA02	A7
NAND_DATA03	J2.110	CPU.NAND_DATA03	D6

Pin Name	Pin	Internal Connections	Ball/pin #
NAND_DATA04	J2.112	CPU.NAND_DATA04	C6
NAND_DATA05	J2.114	CPU.NAND_DATA05	B6
NAND_DATA06	J2.116	CPU.NAND_DATA06	A6
NAND_DATA07	J2.118	CPU.NAND_DATA07	A5

6.2 Variant base peripherals

6.2.1 FULL GPIO configuration

The i.MX6UL GPIO module provides general-purpose pins that can be configured as either inputs or outputs, for connections to external devices. In addition, the GPIO peripheral can produce CORE interrupts.

The device contains 5 GPIO blocks and each GPIO block is made up to 32 identical channels. The device GPIO peripheral supports up to 124 3.3-V GPIO pins. Each channel must be properly configured, since GPIO signals are multiplexed with other interfaces signals. For more information on how to configure and use GPIOs, please refer to section 5.6. For additional details, please refer to chapter 26 of the i.MX6UL APRM Rev.1.

6.3 HMI configuration – use case 1

The following scenario shows a possible example of an HMI appliance where the User Interface is the most important functionality. The LCD controller and the touchscreen controller are the main interfaces used for the HMI interaction.

In the paragraph below you can find a possible peripherals' configuration list that configure the system as an HMI

Remember that some standard peripherals in the list above are required to configure your system.

This configuration suppose to use:

- LCD controller with Backlight PWM
- touchscreen controller interfaced via I2C or SPI peripherals
- 4x4 matrix keypad
- ethernet controller for remote connection (Ethernet on Invariant base)
- up to four UARTs for interfacing to the actuators to be controlled
- synchronous audio interface SAI for external codec (I2S or AC97)
- SD interface for recovery ans storage (SD1 on Invariant base)
- NOR flash for boot and NAND flash for root file system (NOR and NAND on Invariant base)

6.3.1 LCD controller

The I.MX6UL integrates an LCD Controller which provides support for up to 24-bit data output (RGB, 8 bits-per-pixel) and up to WXGA (1366x768) resolution at 60Hz.

It can drive a wide range of devices with different size and capability.

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
LCD_DATA_ENABLE	J2.124	CPU.LCD_DATA_ENABLE	B8
LCD_RESET	J2.126	CPU.LCD_RESET	E9
LCD_VSYNC	J2.128	CPU.LCD_VSYNC	C9

Pin Name	Pin	Internal Connections	Ball/pin #
LCD_HSYNC	J2.130	CPU.LCD_HSYNC	D9
LCD_CLK	J2.132	CPU.LCD_CLK	A8
LCD_DATA00	J2.134	CPU.LCD_DATA00	B9
LCD_DATA01	J2.136	CPU.LCD_DATA01	A9
LCD_DATA02	J2.138	CPU.LCD_DATA02	E10
LCD_DATA03	J2.140	CPU.LCD_DATA03	D10
LCD_DATA04	J2.142	CPU.LCD_DATA04	C10
LCD_DATA05	J2.144	CPU.LCD_DATA05	B10
LCD_DATA06	J2.148	CPU.LCD_DATA06	A10
LCD_DATA07	J2.150	CPU.LCD_DATA07	D11
LCD_DATA08	J2.152	CPU.LCD_DATA09	B11
LCD_DATA09	J2.154	CPU.LCD_DATA10	A11
LCD_DATA10	J2.156	CPU.LCD_DATA11	E12
LCD_DATA11	J2.158	CPU.LCD_DATA12	D12
LCD_DATA12	J2.160	CPU.LCD_DATA13	C12
LCD_DATA13	J2.162	CPU.LCD_DATA14	B12
LCD_DATA14	J2.166	CPU.LCD_DATA14	A12
LCD_DATA15	J2.168	CPU.LCD_DATA15	D13
LCD_DATA16	J2.170	CPU.LCD_DATA16	C13
LCD_DATA17	J2.172	CPU.LCD_DATA17	B13
LCD_DATA18	J2.174	CPU.LCD_DATA18	A13
LCD_DATA19	J2.176	CPU.LCD_DATA19	D14
LCD_DATA20	J2.178	CPU.LCD_DATA20	C14
LCD_DATA21	J2.180	CPU.LCD_DATA21	B14
LCD_DATA22	J2.182	CPU.LCD_DATA22	A14
LCD_DATA23	J2.184	CPU.LCD_DATA23	B16
BL_PWM	J2.46	CPU.CSI_VSYNC	F2

6.3.2 ECSPI2

Pin Name	Pin	Internal Connections	Ball/pin #
ECSPI2_SCLK	J2.74	CPU.CSI_DATA00	E4
ECSPI2_MOSI	J2.76	CPU.CSI_DATA03	E2
ECSPI2_MISO	J2.78	CPU.CSI_DATA02	E1
ECSPI2_CS0	J2.80	CPU.CSI_DATA01	E3

6.3.3 I²C2

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
I2C2_SCL	J2.38	CPU.GPIO1_IO00	K13
I2C2_SDA	J2.48	CPU.GPIO1_IO01	L15

6.3.4 KPP

The following table describes the interface signals:

Pin Name	Pin	Internal Connections	Ball/pin #
KPP_COL4	J2.93	CPU.ENET_RDATA1	C16
KPP_ROW4	J2.95	CPU.ENET_RDATA0	C17
KPP_COL5	J2.97	CPU.ENET_TDATA0	A15
KPP_ROW5	J2.99	CPU.ENET_RXEN	B17
KPP_ROW7	J2.101	CPU.ENET_TX_CLK	D17
KPP_COL7	J2.103	CPU.ENET_RX_ER	D16
KPP_COL6	J2.105	CPU.ENET_TX_EN	B15
KPP_COL6	J2.107	CPU.ENET_TDATA1	A16

6.3.5 UART1

Pin Name	Pin	Internal Connections	Ball/pin #
UART1_TX_DATA	J2.187	CPU.UART1_TX_DATA	K14
UART1_RX_DATA	J2.189	CPU.UART1_RX_DATA	K16

6.3.6 UART2

Pin Name	Pin	Internal Connections	Ball/pin #
UART2_TX_DATA	J2.42	CPU.UART2_TX_DATA	J17
UART2_RX_DATA	J2.44	CPU.UART2_RX_DATA	J16
UART2_RTS	J2.179	CPU.UART2_RTS	H14
UART2_CTS	J2.181	CPU.UART2_CTS	J15

6.3.7 UART3

Pin Name	Pin	Internal Connections	Ball/pin #
UART3_TX_DATA	J2.191	CPU.UART3_TX_DATA	H17
UART3_RX_DATA	J2.193	CPU.UART3_RX_DATA	H16
UART3_CTS	J2.195	CPU.UART3_CTS	H15
UART3_RTS	J2.197	CPU.UART3_RTS	G14

6.3.8 SAI2

Codec reset and IRQ can be connected to any GPIO.

Pin Name	Pin	Internal Connections	Ball/pin #
SAI_TX_BCLK	J2.66	CPU.JTAG_TDI	N16
SAI_TX_DATA	J2.68	CPU.JTAG_TRST	N14
SAI_TX_SYNC	J2.70	CPU.JTAG_TDO	N15
SAI_RX_DATA	J2.72	CPU.JTAG_TCK	M14
SAI_MCLK	J2.34	CPU.JTAG_TMS	P14

6.4 IoT Gateway – use case 2

The following scenario shows a possible example of a blind appliance where Connectivity is the most important functionality. The two ethernet controllers, two USB ports, eight UARTs, two I2C, two SPI and one audio peripherals can be used simultaneously into the Gateway pinmuxing application.

In the paragraph below you can find a possible peripherals' configuration list that configure the system as an IoT Gateway.

Remember that some standard peripherals in the list above are required to configure your system.

This configuration suppose to use:

- enet1 (eth1) ethernet port (Ethernet on Invariant base)
- enet2 ethernet port
- two USB host ports (USB on Invariant base)
- eight UART peripherals
    - four two-wire UART
    - four four-wire UART
- two I2C peripherals
- two SPI peripherals
- SD interface for recovery and storage (SD1 on Invariant base)
- NOR flash for boot (NOR on Invariant base)
- NAND flash (NAND on Invariant base)
    - alternative eMMC (SD2) for root file system
- up to 20 free GPIOs

6.4.1 ENET2

The second ethernet interface requires an external PHY on the Carrier board.

Pin Name	Pin	Internal Connections	Ball/pin #
ENET2_RX_DATA1	J2.93	CPU.ENET_RDATA1	C16
ENET2_RX_DATA0	J2.95	CPU.ENET_RDATA0	C17
ENET2_TX_DATA0	J2.97	CPU.ENET_TDATA0	A15
ENET2_RX_EN	J2.99	CPU.ENET_RXEN	B17
ENET2_TX_CLK	J2.101	CPU.ENET_TX_CLK	D17
ENET2_RX_ER	J2.103	CPU.ENET_RX_ER	D16
ENET2_TX_EN	J2.105	CPU.ENET_TX_EN	B15
ENET2_TX_DATA1	J2.107	CPU.ENET_TDATA1	A16
ENET_MDIO	J2.127	CPU.GPIO_IO06	K17
ENET_MDC	J2.129	CPU.GPIO_IO07	L16

6.4.2 UART1

Pin Name	Pin	Internal Connections	Ball/pin #
UART1_TX_DATA	J2.187	CPU.UART1_TX_DATA	K14
UART1_RX_DATA	J2.189	CPU.UART1_RX_DATA	K16

6.4.3 UART2 – four wires

Pin Name	Pin	Internal Connections	Ball/pin #
UART2_TX_DATA	J2.42	CPU.UART2_TX_DATA	J17
UART2_RX_DATA	J2.44	CPU.UART2_RX_DATA	J16
UART2_RTS	J2.179	CPU.UART2_RTS	H14
UART2_CTS	J2.181	CPU.UART2_CTS	J15

6.4.4 UART3 – four wires

Pin Name	Pin	Internal Connections	Ball/pin #
UART3_TX_DATA	J2.191	CPU.UART3_TX_DATA	H17
UART3_RX_DATA	J2.193	CPU.UART3_RX_DATA	H16
UART3_CTS	J2.195	CPU.UART3_CTS	H15
UART3_RTS	J2.197	CPU.UART3_RTS	G14

6.4.5 UART4 – for wires

Pin Name	Pin	Internal Connections	Ball/pin #
UART4_RX_DATA	J2.124	CPU.LCD_DATA_EN	B8
UART4_CTS	J2.126	CPU.LCD_RESET	E9
UART4_RTS	J2.128	CPU.LCD_VSYNC	C9
UART4_TX_DATA	J2.130	CPU.LCD_HSYNC	D9

6.4.6 UART 5

Pin Name	Pin	Internal Connections	Ball/pin #
UART5_RX_DATA	J2.65	CPU.UART5_RX_DATA	G13
UART5_TX_DATA	J2.67	CPU.UART5_TX_DATA	F17

6.4.7 UART 6

Pin Name	Pin	Internal Connections	Ball/pin #
UART6_RX_DATA	J2.51	CPU.CSI_PIXCLK	E5
UART6_TX_DATA	J2.53	CPU.CSI_MCLK	F5

6.4.8 UART 7

Pin Name	Pin	Internal Connections	Ball/pin #
UART7_TX_DATA	J2.170	CPU.LCD_DATA16	C13
UART7_RX_DATA	J2.172	CPU.LCD_DATA17	B13

6.4.9 UART 8 – for wires

Pin Name	Pin	Internal Connections	Ball/pin #
UART8_TX_DATA	J2.178	CPU.LCD_DATA20	C14
UART8_RX_DATA	J2.180	CPU.LCD_DATA21	B14
UART8_CTS	J2.142	CPU.UART8_CTS	C10
UART8_RTS	J2.144	CPU.UART8_RTS	B10

6.4.10 I²C3

Pin Name	Pin	Internal Connections	Ball/pin #
I2C3_SDA	J2.134	CPU.LCD_DATA00	B9
I2C3_SCL	J2.136	CPU.LCD_DATA01	A9

6.4.11 I²C4

Pin Name	Pin	Internal Connections	Ball/pin #
I2C4_SDA	J2.136	CPU.LCD_DATA02	E10
I2C4_SCL	J2.138	CPU.LCD_DATA03	D10

6.4.12 ECSPI2

Pin Name	Pin	Internal Connections	Ball/pin #
ECSPI2_SCLK	J2.74	CPU.CSI_DATA00	E4

Pin Name	Pin	Internal Connections	Ball/pin #
ECSPI2_MOSI	J2.76	CPU.CSI_DATA03	E2
ECSPI2_MISO	J2.78	CPU.CSI_DATA02	E1
ECSPI2_CS0	J2.80	CPU.CSI_DATA01	E3

6.4.13 ECSPI3

Pin Name	Pin	Internal Connections	Ball/pin #
ECSPI3_CS0	J2.84	CPU.NAND_READY#	A3
ECSPI3_MISO	J2.86	CPU.NAND_CLE	A4
ECSPI3_SCLK	J2.96	CPU.NAND_CS0#	C5
ECSPI3_MOSI	J2.98	CPU.NAND_CS1#	B5

6.4.14 MMC/SD/SDIO2

If an external eMMC is required, it can be mapped on the following pin list (instead of using internal NAND):

Pin Name	Pin	Internal Connections	Ball/pin #
SD2_RESET	J2.88	CPU.NAND_ALE	B4
SD2_CLK	J2.90	CPU.NAND_RE#	D8
SD2_CMD	J2.92	CPU.NAND_WE#	C8
SD2_DATA0	J2.104	CPU.NAND_DATA00	D7
SD2_DATA1	J2.106	CPU.NAND_DATA01	B7
SD2_DATA2	J2.108	CPU.NAND_DATA02	A7
SD2_DATA3	J2.110	CPU.NAND_DATA03	D6
SD2_DATA4	J2.112	CPU.NAND_DATA04	C6
SD2_DATA5	J2.114	CPU.NAND_DATA05	B6
SD2_DATA6	J2.116	CPU.NAND_DATA06	A6
SD2_DATA7	J2.118	CPU.NAND_DATA07	A5

6.5 Customized pin muxing configuration

Customers can require any other multiplexing contacting the DAVE Embedded Systems' sales department at sales@dave.eu .

Please contact your sales representative for assistance on pin multiplexing design.

Additionally, for Evaluation Kit owners is available on the DAVE Embedded Systems' Reserved Area a pin muxing excel sheet which simplify the pin muxing configuration

7 Power, reset and control

AXEL ULite system-on-module (SOM for short) is powered by carrier board via VIN_SOM rail.

About voltage range, three supported configurations are available. These configurations are indicated by the value of the **f** field of the ordering code. The generic ordering code is in the form:

DA p l r n c f t s

The field **f** can assume the following values:

- 0,1: power supply voltage range 3.135 - 3.465V (that is 3V3±5%)
- 2: power supply voltage range is 3.3 - 4.5V
  - please note that this range can be widened by the use of an external MOSFET; for more details please refer to technical support
- 3: power supply voltage range is 3.25 - 3.465V (that us 3.3 +5%/-1.5%).

Voltage references for single-ended I/O signals the same for all configurations. They are detailed in the following table.

Signal groups	Voltage reference	SODIMM pin number	Nominal voltage
UART1-UART5 CSI LCD NAND SD1 JTAG GPIO1 ENET1-ENET2	3V3_IO	155	3.3
SNVS_TAMPER[9:0]	VDD_SNVS_IN	143	3.0

What is interfaced to 3.3V signals at carrier board level may be referenced to a different voltage than 3.3V_IO. However, the difference

between this voltage and 3.3V_IO must not exceed 300mV.

This constraint is automatically satisfied if

- one of the following ordering codes is used: DAplrnc0ts, DAplrnc1ts or DAplrnc3ts
- the same voltage rail is used to power **AXE ULite** SOM and 3.3V carrier board circuitry.

Since powering is strictly related to reset signals, reading of this page is highly recommended.

For information about power consumption, please refer to this article.

7.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for i.MX6UL processors is not a trivial task because several power rails are involved. **AXEL ULite** SOM simplifies this task by embedding all the needed circuitry. The following picture shows a simplified block diagram of PSU/voltage monitoring circuitry:

The following picture shows a simplified block diagram of PSU/voltage monitoring circuitry:

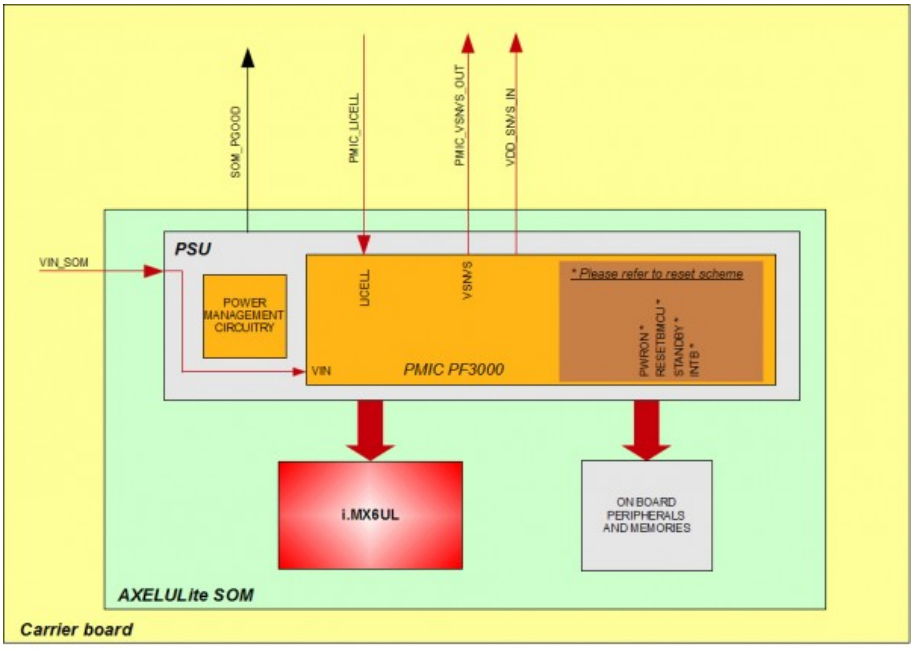

Fig. 5: Simplified block diagram of integrated power supply unit

The PSU is composed of two main blocks:

- power management integrated circuit (PMIC, NXP PF0100E0 - on request this part is available in automotive grade)
- additional generic power management circuitry that completes PMIC functionalities.

The PSU:

- generates the proper power-up sequence required by i.MX processor and surrounding memories and peripherals
- synchronizes the powering up of carrier board in order to prevent back power
- provides some spare regulated voltages that can be used to power carrier board devices

7.1.1 Power-up sequence

The typical power-up sequence is the following:

1. (optional) PMIC_LICELL is powered by a Lithium coin cell battery
   - I.MX6 UL SNVS domain is powered (VDD_SNVS_IN)
2. VIN_SOM main power supply rail is powered
   - I.MX6 UL SNVS domain is powered (VDD_SNVS_IN)
3. CPU_PORn (active-low) is driven low
4. PMIC_PWRON signal is pulled-up (unless carrier board circuitry keeps this signal low for any reason)
5. PMIC transitions from OFF to ON state
6. PMIC initiates power-up sequence as per I.MX6 UL requirements
7. SOM_PGOOD signal is set ti logic '1'; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa). Generally speaking, all the circuitry that interfaces SOM's I/O signals should be powered on when SOM_PGOOD turns to logic '1'.
8. CPU_PORn is released.

For further details, please refer to[2],[3]

2 Freescale Semiconductor, PF3000 Advance Information - Power Management Integrated Circuit (PMIC) for i.MX 7 & i.MX 6SL/SX/UL

3 Freescale Semiconductor, Data Sheet: Technical Data - i.MX 6UltraLite Applications Processors for Industrial Products

7.2 Reset scheme and control signals

The following picture shows the simplified block diagram of reset scheme and voltage monitoring.

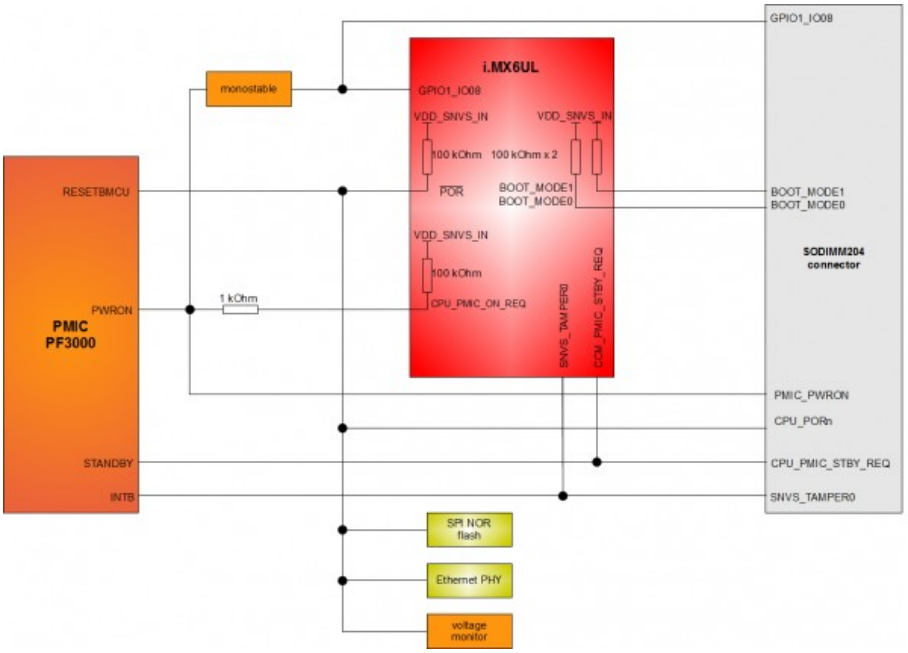

Fig. 6: Simplified block diagram of reset circuitry and voltage monitoring

The available reset signals are described in detail in the following sections.

7.2.1 CPU_PORn

The following devices can assert this active-low signal:

- PMIC
- voltage monitor: this device monitors critical power voltages and triggers a reset pulse in case any of these exhibits a brownout condition.

Since SPI NOR flash can be used as boot device, CPU_PORn is connected to this device too. This guarantees it is in a known state when

reset signal is released.

7.3 System boot

NXP i.MX6UL processor implements a very flexible boot process. This versatility comes at the price of a non trivial bootstrap configuration scheme. Typical system-on-module (SOM for short) adopter does not need to deal with such a complexity. In other words, he/she expects to manage few boot configuration issues because it is assumed that most of them are "hidden" within the SOM itself. Nevertheless, there are specific applications where the system integrator needs full control of all the bootstrap configuration options, even if the design is built upon a SOM.

These two needs - ease of use and configurability - clearly push in opposite directions. During the inception of the **AXEL ULite** product, specific attention has been addressed to find a viable trade off to satisfy such requirements. This effort has led to the options that are detailed in the section Options for users. Reader can skip directly to this paragraph, however he/she is encouraged to read this section as well, in order to get an overview of the processor's boot process.

It is worth remembering that an exhaustive discussion of this issue is beyond the scope of this article. For more details, please refer to [4]

7.3.1 Boot options

Please, keep BOOT_MODE1 = '0' for standard boot mode usage. For further information on boot options, please contact the Technical Support Team.

7.3.1.1 SPI NOR / SD option

BOOT_MODE0	0	1 or floating
Primary boot device	NOR	SD
Fallback	-	USB serial downloader

Tab. 20: SPI NOR / SD option

4 NXP, IMX6ULRM, *i.MX 6UltraLite Applications Processor Reference Manual*

7.3.1.2 NAND / SD option

Not available on actual AxelULite SOM.

BOOT_MODE0	0	1 or floating
Primary boot device		
Fallback		

Tab. 21: NAND / SD option

7.4 Clock scheme

This section will be completed in a future version of this manual.

7.5 Recovery

For different reason, starting from image corruption due power loss during upgrade or unrecoverable bug while developing a new U-Boot feature, the user will need, sooner or later, to recover (bare-metal restore) the **AXEL ULite** SOM without using the bootloader itself. The following paragraphs introduce the available options.

For further information, please refer to DAVE Embedded Systems Developers Wiki or contact the Technical Support Team.

7.5.1 JTAG Recovery

JTAG recovery, though very useful (especially in development or production environment), requires dedicated hardware and software tools. **AXEL ULite** provides an internal connector for the JTAG interface, which, besides the debug purpose, can be used for programming and recovery operations.

For further information on how to use the JTAG interface, please contact the Technical Support Team.

7.5.2 USB Recovery

The USB Serial Downloader provides a means to download the bootloader image to the chip over USB serial connection.

Please refer to the XUELK Quick Start Guide for further details.

7.5.3 SD/MMC Recovery

MMC recovery is a valuable options that requires no special hardware at all, apart a properly formatted MMC. When SD/MMC boot option is selected, bootrom looks for a valid bootloader on SD/MMC. Once the board is running after booting from SD, reprogramming the flash memory is straightforward. The SD peripheral used for boot is MMC/SD/SDIO1 (please refer to 6.1.3.1).

7.6 Multiplexing

Most of the i.MX6UL processor pins have multiple signal options. These signal to pin and pin to signal options are selected by the input output multiplexer called IOMUX. The IOMUX enables flexible IO multiplexing and is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis. Each IO pad has default and up to seven alternate functions, which are software configurable.

Please refer to the following sections of the i.MX6UL APRM for further information pin assignment:

- chapter 4 “External Signals and Pin Multiplexing”
- section 4.1 “Pin assignments”
- section 4.2 “Muxing options”
- chapter 36 “IOMUX Controller (IOMUXC)”

8 Operational characteristics

This section describes the operational characteristics including:

- PSU input range that can be configured in several ways
- Power consumption
- Heat dissipation

8.1 PSU input range

8.1.1 PSU input configuration 0,1

Parameter	Min	Typ	Max	Unit
Main power supply voltage	3.135	3.3	3.465V	

8.1.2 PSU input configuration 2

Parameter	Min	Typ	Max	Unit
Main power supply voltage	3.3	3.7	4.5V	

8.1.3 PSU input configuration 3

Parameter	Min	Typ	Max	Unit
Main power supply voltage	3.25	3.3	3.465V	

8.2 Power consumption

Providing theoretical maximum power consumption value would be useless for the majority of system designers building their application upon **AXEL ULite** module because, in most cases, this would lead to an over-sized power supply unit. Several configurations have been tested in order to provide figures that are measured on real-world use cases instead. Please note that **AXEL ULite** platform is so flexible that it is virtually impossible to test for all possible configurations and applications on the market. The use cases here presented should cover most of real-world scenarios. However actual customer application might require more power than values reported here. Generally speaking, application specific requirements have to be taken into consideration in order to size power

supply unit and to implement thermal management properly.

8.2.1 Configuration1

This section will be completed in a future version of this manual.

8.3 Heat Dissipation

This section will be completed in a future version of this manual.

9 Application Notes

Please refer to the following documents available on DAVE Embedded Systems Developers Wiki:

Document	Location

Tab. 22: Application Notes

10 RESERVED AREA registration

Additional development kit contents, binary images and documentation can be downloaded from the RESERVED AREA of the DAVE Embedded Systems' website. Registering the development kit is required to get access to the RESERVED AREA. The procedure is the following:

- purchase the development kit (please contact sales@dave.eu for further details)
- send the product information to the sales department (sales@dave.eu)
- the sales department will create the account and enable access to the RESERVED AREA
- the sales department will send the credentials to the customer

The customer can then access the RESERVED AREA from the DAVE Embedded Systems' web site home page, clicking on the "**SUPPORT->Reserved Area**" entry from the top menù, or clicking on the dedicated button in the lower section of the page.

Fig. 7: Accessing the RESERVED AREA