DAVE Embedded Systems

AN-BELK-004: Interfacing BoraEVB to TFT LCD display

Application Note

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Application Note

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1 Introduction

Zynq-7000 series from Xilinx are not equipped with a LCD output nor – consequently - with a LCD controller.
But if you want to provide a LCD interface to your Zynq-based design, many IP's are available for that purpose both from the Open Source world, and commercial ones.
Beside that, you would need also to provide your design with a physical link between your Zynq and the LCD.

This application note describes how to interface a popular LCD display model (Ampire AM-800480STMQW-TA1) to DAVE Embedded Systems' BoraEVB starting from the availability of a LCD controller in its Zynq-based engine. LCD controller is not described in detail since it may vary with customers' needs. Also, small variants as color depth and spatial resolution, may be easily adapted by readers.

This project is based on BELK 2.2.0. that is last release of BORA Development Kit. Since BELK is based on Vivado, a sample code for Vivado is released.

All details on our WIKI at this link.

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2 Physical interfacing

Main characteristics of this popular 7" TFT LCD panel are:

- 800x480 resolution
- color depth: 18 bpp
- electrical interface: LVDS (3 pairs).

To interface the display with respect to the BoraEVB, a small *adapter board* is needed. It interfaces J22 connector on BoraEVB side and provides a 20-pin connector to directly attach display cable.

The *adapter board*:

- is also equipped with a linear regulator generating 2.5V. This voltage is used as power supply for the VDDIO_BANK13 rail. This voltage is required to implement LVDS differential pairs that drive display.
- integrates a pad (denoted as TP1) that is used to connect 5V power supply generated by MOD2 PSU of BoraEVB. This additional power rails is required by display backlight circuitry.

Ampire AM-800480STMQW-TA1 part integrates resistive touch too. This is directly connected to BoraEVB's J25 connector. Resistive touch is managed by Texas Instruments TSC2003 controller (U27).

Schematics of adapter board can be downloaded from this link[1].

1 This link refers to DAVE Embedded Systems' RESERVED AREA. In order to access to the area, please be free to contact sales@dave.eu

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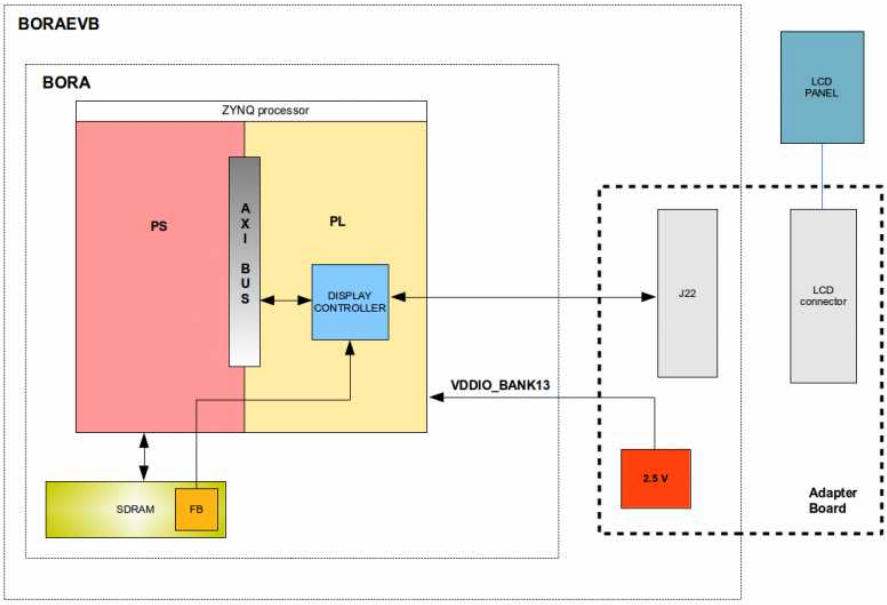
3 Block diagram and Vivado project

The following picture shows simplified block diagram of the design.



LCD is driven by a controller implemented in PL that fetches pixel data from frame buffer and periodically refreshes physical screen. The LCD controller is composed of an *AXI VDMA*[2] IP, the LCD controller itself and a parallel-to-LVDS serializer. AXI VDMA and the LCD controller provides configuration registers that are mapped in the following address range:

- AXI VDMA: 0x43000000 - 0x4300FFFF
- LCD Controller: 0x43C00000 - 0x43C0FFFF

2 By Digilent

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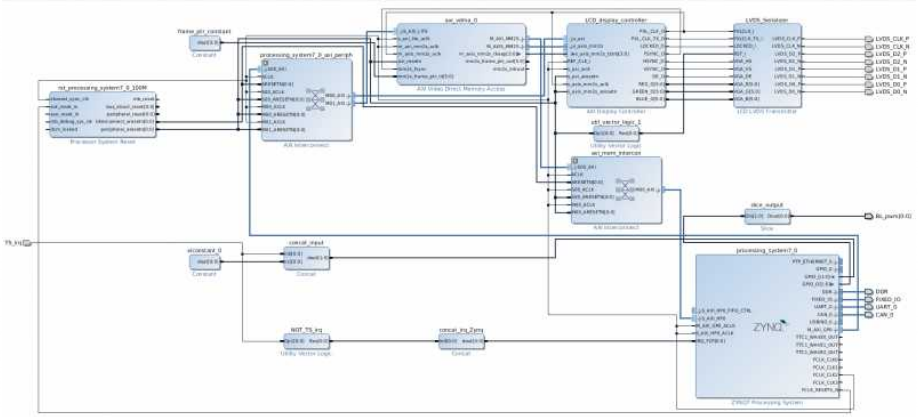
The following picture shows the block diagram of the Vivado project with LCD controller:



To implement frame buffer, a portion of main SDRAM is used. This area is allocated at runtime by linux frame buffer driver. Even if LCD is 18 bpp, each pixel is represented by 32-bit word in memory. In fact each pixel is in RGB666 format, so for each colour only the six most significant bits of the frame buffer RGB888 are used to drive the display.

Here is the pinout assignment to drive the LCD:

LCD Signal	BORA SOM Signal
BackLight (*)	IO_L15P_T2_DQS_13
LVDS_CLK_P	IO_L22P_T3_13
LVDS_CLK_N	IO_L22N_T3_13
LVDS_D0_P	IO_L21P_T3_DQS_13
LVDS_D0_N	IO_L21N_T3_DQS_13
LVDS_D1_P	IO_L19P_T3_13

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LVDS_D1_N	IO_L19N_T3_VREF_13
LVDS_D2_P	IO_L18P_T2_13
LVDS_D2_N	IO_L18N_T2_13

The Vivado project can be downloaded from this link[3].

(*) This signal is used to control backlight. It is usually driven by a PWM signal whose duty cycle is proportional to backlight intensity. For the sake of simplicity, in this project this signal is driven by a GPIO, thus only two intensity levels are supported (0% and 100%).

4 Enabling frame buffer driver in linux kernel

To enable frame buffer driver user has to:

- get the pre-built binaries here[4].

Kernel and device tree can also be built with the following procedure:

- update Bora kernel repository (as described here)
- checkout bora-feat-lcd-support branch (using git checkout bora-feat-lcd-support command)
- build the updated kernel source as usual.

Put the binaries on the first (FAT32) partition of your BELK 2.2.0 SD card, overwriting the original one if needed. Please note that

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you need the following files:

- boot.bin
- bora.dtb
- uImage
- fpga.bin
- uEnv.txt

Insert the SD card into BoraEVB and turn on the board.

During kernel bootstrap, the following messages are printed out on console, indicating framebuffer driver has been loaded succesfully:

```
[    0.600840] borafb borafb.0: fb0: Virtual frame buffer
device, using 16384K of video memory @ phys 2d900000
```

You will also see two Tuxes on the top left corner of the LCD, indicating that this Linux system has two cores, as shown in the following picture:

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Once the kernel has completed boot, frame buffer can be accessed from user space applications via /dev/fb0 device file (for more details please refer to https://www.kernel.org/doc/Documentation/fb/framebuffer.txt).

The following picture shows Qt 4.8.3 Affine Transformations demo application running on top of it.

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