

AN-BELK-003: Interfacing DDR3 SDRAM to PL

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1 Introduction

CPU modules are characterized by direct addressing of hardware resources: NOR, NAND and RAM. BORA CPU module is not an exception.

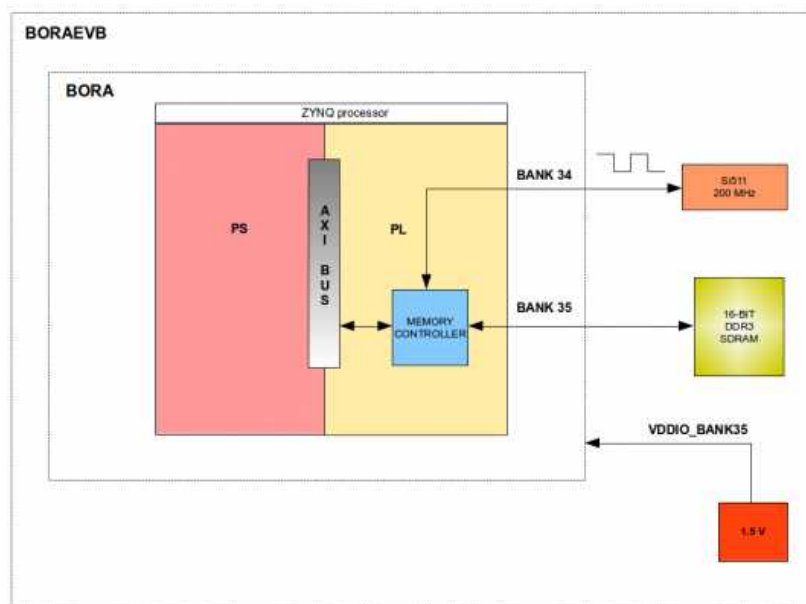
However it might be useful to be able to address also a *secondary* RAM as an example to be used as a buffer or graphic memory. To achieve that, users need to design an IP in PL part of Zynq and reserve a dedicated bank in FPGA in order to have exclusive access and to maximize bandwidth. In any case, since this additional SDRAM bank is accessible via AXI bus, it is mapped in the processor's memory space and thus it can be accessed by PS as well.

BoraEVB can optionally be populated with a 16-bit 512MB SDRAM chip that is directly connected to PL (1). This application note describes how to enable the support for this additional memory bank. An example Vivado design is released along with this application note, based on [BELK 2.1.0](#) ¹

¹ For more information about this option, please contact technical support (support-bora@dave.eu)

2 Physical interfacing

The following picture shows logical connection of the SDRAM bank.

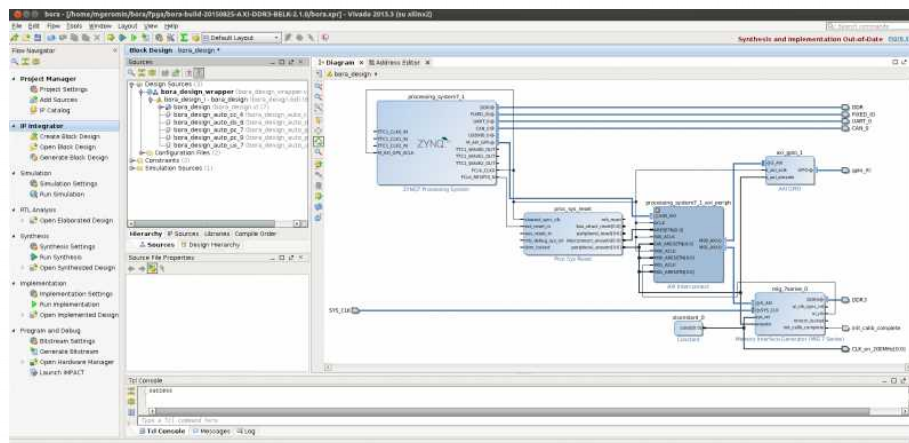


Please note that the BANK #35 of Zynq must be powered at 1.5V to interface DDR3 SDRAM. To do that J11.1-2 must be opened and J11.3-4 must be shorted.

3 Integrating memory controller

As depicted in the block diagram below, a memory controller has to be instantiated in PL to access SDRAM. This block has been generated with Memory Interface Generator (MIG) tool (<http://www.xilinx.com/products/intellectual-property/mig.html>).

Memory Interface Generator (MIG) is configured properly to work with Micron MT41K64M16JT-15E DDR3 memory chip at the frequency of 400MHz. It needs a precise external reference clock of 200MHz provided by an active LVDS oscillator connected on BANK #34 pins. The MIG is then connected to the PS through the AXI GP0 interface to allow user to access the external memory.



The Vivado example project can be downloaded from the following URL:

[AN-BELK-003 Vivado project \(without synthesis and implementation results\)](#)²

² This link refers to DAVE Embedded Systems' RESERVED AREA. In order to access to the area, please be free to contact sales@dave.eu

This project requires a 200 MHz clock source. It has been tested with

- Silicon Labs Si511BBA200M000BAG active oscillator populating reference XO1 on BoraEVB
- Micron MT41K64M16JT-15E DDR3 chip running at 400 MHz.

The bitstream and boot binaries can be downloaded from the following area:

[AN-BELK-003 binaries](#)³

4 SDRAM bank mapping

SDRAM bank is mapped in the PS's addressable space at physical address range 0x48000000-0x4FFFFFFF, as shown in the following picture:



Cell	Interface Pin	Base Name	Offset Address	Range	High Address
processing_system7_1					
Data (32 address bits : 4G)					
mig_7series_0	S_AXI	memaddr	0x48000000	128M	0x4FFFFFFF
axi_gpio_1	S_AXI	Reg	0x41200000	64K	0x4120FFFF

The following dump shows a simple memory test run from U-Boot console:

```
U-Boot 2013.04 (Aug 25 2014 - 23:52:57) [belk-2.1.0]

I2C:   ready
Memory: ECC disabled
DRAM:  1 GiB
WARNING: Caches not enabled
Now running in RAM - U-Boot at: 3ff68000
NAND:  1024 MiB
```

³ This link refers to DAVE Embedded Systems' RESERVED AREA. In order to access to the area, please be free to contact sales@dave.eu

```

MMC:   zynq_sdhci: 0
SF: Detected S25FL256S_64K with page size 64 KiB, total
32 MiB
In:    serial
Out:   serial
Err:   serial
Net:   Gem.e000b000
Hit any key to stop autoboot:  0
zynq-uboot> help mtest
mtest - simple RAM read/write test

Usage:
mtest [start [end [pattern [iterations]]]]
zynq-uboot>
zynq-uboot> mtest 0x48000000 0x4FFFFFFF
Testing 48000000 ... 4fffffff:
Pattern 00000000 Writing... Reading...Iteration:      53
zynq-uboot> <INTERRUPT>
zynq-uboot>
zynq-uboot> mtest 0x48000000 0x4FFFFFFF 0xA5A5A5A5
Testing 48000000 ... 4fffffff:
Pattern A5A5A5A5 Writing... Reading...Iteration:      19
zynq-uboot> <INTERRUPT>

```

It's also possible to extend Linux kernel memory with the external memory adding a second memory in the device tree:

```

axi_dds: memory@48000000 {
    device_type = "memory";
    reg = < 0x48000000 0x08000000 >;
};

```

The kernel patch can be downloaded from following URL:

[AN-BELK-003 Linux patch](#)⁴

4 This link refers to DAVE Embedded Systems' RESERVED AREA. In order to access to the area, please be free to contact sales@dave.eu