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# PPChameleon

## *Hardware Manual*

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## PPChameleon Hardware Manual

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# 1 - Introduction

PPChameleon is a General Purpose microprocessor board powered by PowerPC 405EP processor from IBM.

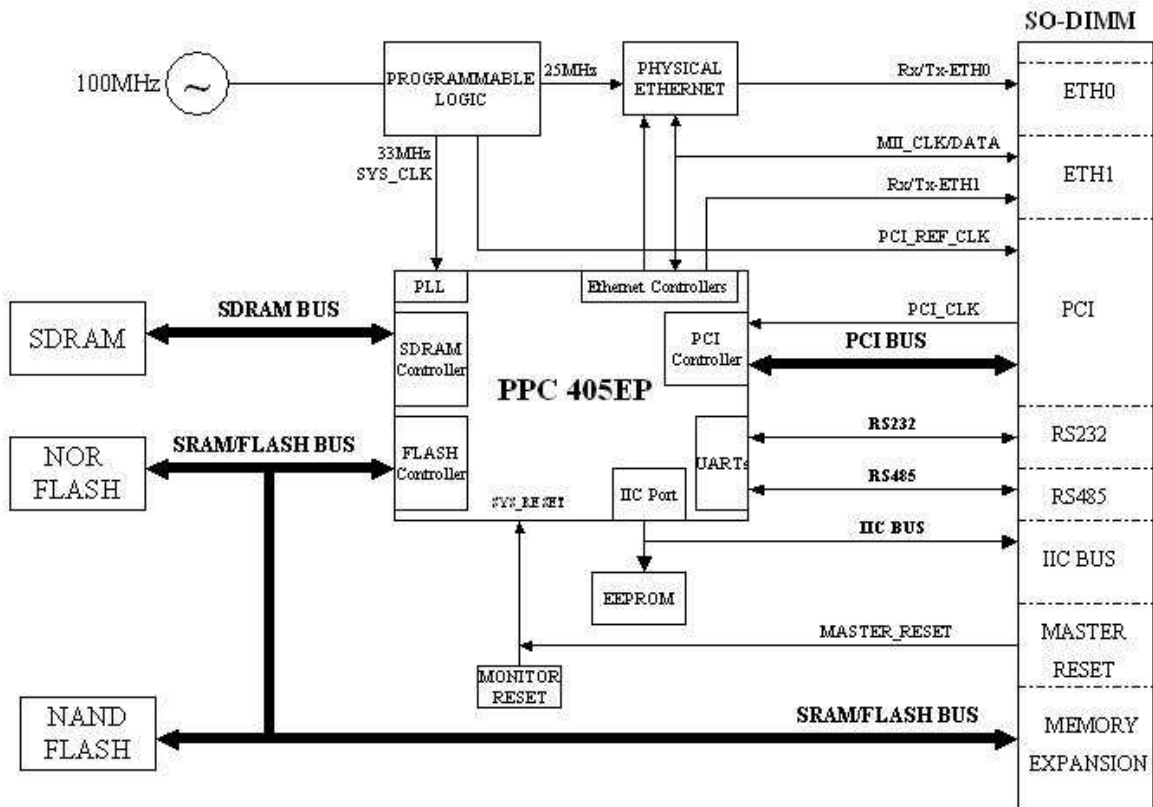
PPChameleon module comes with all essential features needed in order to quickly set up a customized system based on this processor. As an example, module comes with its flash NOR memory and SDRAM memory as well as reset logic, in order to provide proper power-on reset sequence and power monitor.

All interface signals are passed through one DDR-SO DIMM (200 pin) edge connector, therefore users should complete hardware interfaces and connectors when they want to use them through the host board.

A quick overview of the board is given, both from mechanical and electrical point of view. Nevertheless, for detailed information, user should refer to components manufacturer's data sheet.

Other related documents are the PPChameleon Embedded Linux Kit [1] and PPChameleon EVB Evaluation Board User Manual [2].

# 2 - Block Scheme



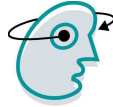


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## 3 - Specifications

All specifications refer to standard productions. For customizations and details, please contact your distributor.

CPU	PowerPC 405EP release C
Speed	133, 266 or 333 MHz
Flash	4 MBytes
RAM	32, 64 or 128 MBytes
EEPROM	16Kbit
NAND	32 [16 or 64] MBytes
Reset	External and CPU supervisor with Master Reset input
Power supply	3.3V and 1.8V supply
Power consumption	800mA [typ] / 1240 mA [worst case]
Weight	20 g
Dimensions	67.5 x 50.8 mm <sup>2</sup> [2.7 x 2.0 inches]
Edge connector	JEDEC Standard No. 21-C, module 4.20.6



## 4 - Board layout and Physical

PPChameleon is designed around a 200 pin “double height” DDR\_SO DIMM JEDEC standard [1][4]. Users should consider that mechanical tolerances are within  $\pm 0.15$  mm.

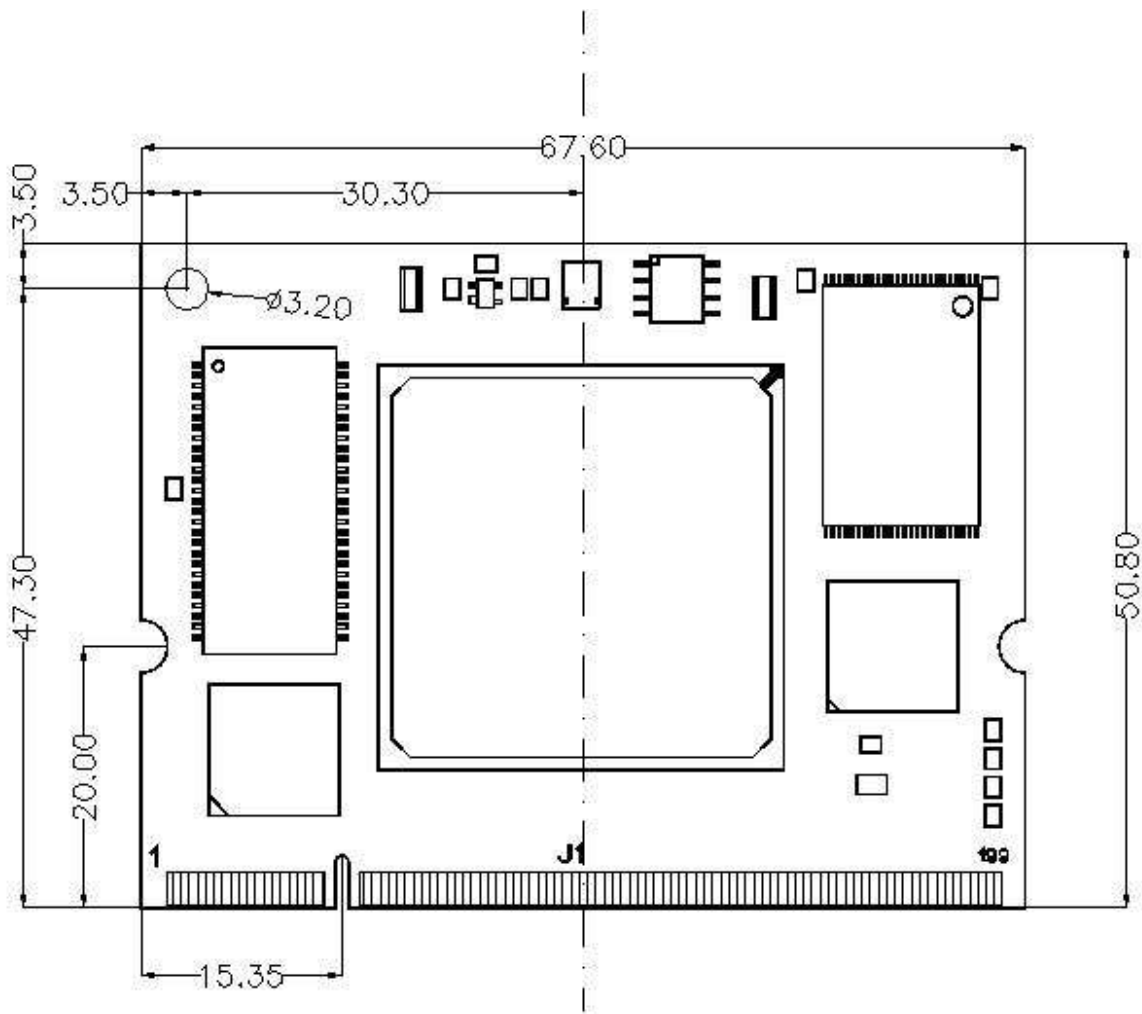


Fig. 1 – PPChameleon board layout



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## 5 - Interfaces, connectors type and pinout

### 5.1 Interfaces

There is only one connector in the board (J1) as depicted in Fig. 1.

J1 is an edge connector mechanically compliant with a JEDEC Standard (No. 21-C, module 4.20.6, see references [3] and [4]).

Where a “standard” connector is used, odd pins are faced up.

### 5.2 Connectors

PCB can mate with different types of connectors, listed below:

- AMP series 1376408-1
- DELPHI series 1543 1499
- JAE series MM50-200
- YAMAICHI IC – 657 – 200 – MF (vertical, for test purposes)

Three main issues must be kept in mind when using these kind of connectors:

- a) Such connectors are conceived to be used as support of SDRAM memory DIMMs, therefore they are homologated for a low number of insertions, usually some handful.
- b) PPChamelon is formally a 2.5V module. In fact it has the *pivot* slot depicted in Fig. 1 in the position typical of a 2.5V module. Insertion in 1.8V connectors is prevented.
- c) Module has been designed to be mated with *standard* type connectors. With standard connectors, microprocessor is face-up and odd-numbered pins are visible. Mating with *reverse* connectors is possible but there is no guarantee about dissipation. In fact – in this case – most components are facing host board and air can not freely circulate.

### 5.3 Pinout

In Tab. 1 connections carried over the connectors J1 are summarized. Names of the signals often remind the names of the microprocessor signals, if they are connected to the microprocessor itself. Only main function is indicated in the Tables below under the column “name”, being several pins available for multiple purposes. In order to know in detail which pins can be used with an alternate function, user should refer to the Data Sheet of the microprocessor manufacturer. Also detailed electrical specifications (levels, tolerances, timings and so on) must be verified on official document released by manufacturer.

**Please, take note that Addresses and Data relative to the Peripheral Bus are annotated with the convention that the zeroed bit is always the Least Significant Bit. That is D0 is the LSB of the Data and A0 is the LSB of the Addresses.**



As a doublecheck, you can verify where the pin is connected to the microprocessor, by looking at the second column (uP pin).

<i>ROW 1 to 99 (odd)</i>			
<i>Pin</i>	<i>uP pin</i>	<i>Name</i>	<i>Description</i>
1		3V3	Output driver supply voltage at 3.3V
3		3V3	Output driver supply voltage at 3.3V
5		3V3	Output driver supply voltage at 3.3V
7		1V8	Logic supply voltage at 1.8V
9		1V8	Logic supply voltage at 1.8V
11		1V8	Logic supply voltage at 1.8V
13		GND	Ground
15		GND	Ground
17		GND	Ground
19		GND	Ground
21		GND	Ground
23		OUT0	25 MHz output for external PHY device (LVTTTL)
25		OUT1	10/100 Mbit led; 100 Mbit when HIGH, 10 Mbit when LOW
27		OUT2	LINK led; stable link is achieved when HIGH, blinks with RX/TX activity
29		OUT3	FD/COL; when HIGH a full duplex detected; blinks with collisions
31	C22	HALT	Halt from external debugger
33		TRST#	JTAG reset; internally pulled up with 10KΩ resistor; connected to a LVCMOS input
35		MRST#	Master reset input; pulled up with a 10KΩ resistor
37	Y02	TCK	JTAG clock; internally pulled up with 10KΩ resistor
39	N02	U0RTS	UART0 Request To Send
41	L04	U0RI	UART0 Ring Indicator; to access this function,software must toggle a DCR bit
43	M04	U0DCD	UART0 Data Carrier Detect; to access this function,software must toggle a DCR bit
45	J01	U0DTR	UART0 Data Terminal Ready; to access this function,software must toggle a DCR bit
47	W20	IO30/ REJP0	External request to reject a packet
49	Y21	IO31/ REJP1	External request to reject a packet
51	AA23	TS1E/NCE#	Even Trace execution status; to access this function,software must toggle a DCR bit; NAND Chip Enable when NAND is on-board
53	Y22	TS2E/NCLE	Even Trace execution status; to access this function,software must toggle a DCR bit; NAND CLE when NAND is on-board
55	Y23	TS1O/NALE	Odd Trace execution status; to access this function,software must toggle a DCR bit; NAND ALE when NAND is on-board
57	W21	TS2O/NRB	Odd Trace execution status; to access this function,software must toggle a DCR bit; NAND RB when NAND is on-board; to be used in this way, it must be externally pulled up with a 4.7kΩ resistor [as in the PPCEVB]
59	U20	TS3	Trace status; to access this function,software must toggle a DCR bit
61	V23	TS4	Trace status; to access this function,software must toggle a DCR bit
63	U21	TS5	Trace status; to access this function,software must toggle a DCR bit
65	U22	TS6	Trace status; to access this function,software must toggle a DCR bit
67	T21	TrcClk	Trace interface clock.Operates at half the CPU core frequency. To access this function,software must toggle a DCR bit. <b>Note:</b> Initialization strapping must hold this pin low (0)during reset.
69	R21	PCIAD31	PCI Address/Data Bus.Multplexed address and data bus.
71	R22	PCIAD30	PCI Address/Data Bus.Multplexed address and data bus.
73	R23	PCIAD29	PCI Address/Data Bus.Multplexed address and data bus.
75	P21	PCIAD28	PCI Address/Data Bus.Multplexed address and data bus.
77	P22	PCIAD27	PCI Address/Data Bus.Multplexed address and data bus.
79	N21	PCIAD26	PCI Address/Data Bus.Multplexed address and data bus.
81	N22	PCIAD25	PCI Address/Data Bus.Multplexed address and data bus.
83	N23	PCIAD24	PCI Address/Data Bus.Multplexed address and data bus.
85	M21	PCIAD23	PCI Address/Data Bus.Multplexed address and data bus.
87	L23	PCIAD22	PCI Address/Data Bus.Multplexed address and data bus.
89	L22	PCIAD21	PCI Address/Data Bus.Multplexed address and data bus.
91	L21	PCIAD20	PCI Address/Data Bus.Multplexed address and data bus.
93	K22	PCIAD19	PCI Address/Data Bus.Multplexed address and data bus.
95	K21	PCIAD18	PCI Address/Data Bus.Multplexed address and data bus.
97	J23	PCIAD17	PCI Address/Data Bus.Multplexed address and data bus.
99	J22	PCIAD16	PCI Address/Data Bus.Multplexed address and data bus.



<i>Pin</i>	<i>uP pin</i>	<i>Name</i>	<i>Description (101 to 199 – odd)</i>
101	H23	PCIPERR#	PCIPERR# is used for reporting data parity errors on PCI transactions.PCIPErr is driven active by the device receiving PCIAD00:31,PCIC3:0/BE3:0,and PCIParity,two PCI clocks following the data in which bad parity is detected.
103	G22	PCISTOP#	The target of the current PCI transaction can assert PCISTO# to indicate to the requesting PCI master that it wants to end the current transaction.
105	F22	PCIFRAME#	PCIFRAME# is driven by the current PCI bus master to indicate the beginning and duration of a PCI access.
107	E22	PCIREQ#2	Bus request from external master.
109	D23	PCIGNT#0	Grant signal to external master requesting the bus
111	E23	PCIGNT#1	Grant signal to external master requesting the bus
113	D14	TXD13	Ethernet interface 1: transmit data
115	A15	TXD12	Ethernet interface 1: transmit data
117	C14	TXD11	Ethernet interface 1: transmit data
119	B15	TXD10	Ethernet interface 1: transmit data
121	C15	TX1ERR	Ethernet interface 1: receive error
123	A16	TX1EN	Ethernet interface 1: transmit enable
125	C06	TX1CLK	Ethernet interface 1: medium transmit clock
127	Y06	MDC	Ethernet interface 0/1: management data clock
129	AA5	MDIO	Ethernet interface 0/1: management data input/output
131	B14	<b>A0 (LSB)</b>	<b>Least Significant Bit</b> of the Address line for peripheral bus
133	A14	A1	Address line for peripheral bus
135	C13	A2	Address line for peripheral bus
137	B13	A3	Address line for peripheral bus
139	A13	A4	Address line for peripheral bus
141	C12	A5	Address line for peripheral bus
143	B12	A6	Address line for peripheral bus
145	D12	A7	Address line for peripheral bus
147	A11	A8	Address line for peripheral bus
149	C11	A9	Address line for peripheral bus
151	A10	A10	Address line for peripheral bus
153	D11	A11	Address line for peripheral bus
155	B10	A12	Address line for peripheral bus
157	C10	A13	Address line for peripheral bus
159	D10	A14	Address line for peripheral bus
161	C9	A15	Address line for peripheral bus
163	A8	A16	Address line for peripheral bus
165	D9	A17	Address line for peripheral bus
167	B8	A18	Address line for peripheral bus
169	C8	A19	Address line for peripheral bus
171	B7	A20	Address line for peripheral bus
173	C7	A21	Address line for peripheral bus
175	D8	A22	Address line for peripheral bus
177	A6	A23	Address line for peripheral bus
179	B6	A24	Address line for peripheral bus
181	D7	A25	Address line for peripheral bus
183	A5	A26	Address line for peripheral bus
185	A4	A27	Address line for peripheral bus
187	B4	<b>A28 (MSB)</b>	<b>Most Significant Bit</b> of the Address line for peripheral bus
189		CTTD	Signal to be routed to the central tap of TX LAN insulation transformer
191		CTRD	Signal to be routed to the central tap of RX LAN insulation transformer
193		RX-	Signal to be routed to the negative pin of RX winding of LAN insulation transformer
195		RX+	Signal to be routed to the positive pin of RX winding of LAN insulation transformer
197		TX+	Signal to be routed to the negative pin of TX winding of LAN insulation transformer
199		TX-	Signal to be routed to the positive pin of TX winding of LAN insulation transformer

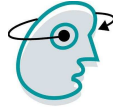


<b>Pin</b>	<b>uP pin</b>	<b>Name</b>	<b>Description (2 to 100 - even )</b>
2		3V3	Output driver supply voltage at 3.3V
4		3V3	Output driver supply voltage at 3.3V
6		3V3	Output driver supply voltage at 3.3V
8		1V8	Logic supply voltage at 1.8V
10		1V8	Logic supply voltage at 1.8V
12		1V8	Logic supply voltage at 1.8V
14		GND	Ground
16		GND	Ground
18		GND	Ground
20		GND	Ground
22		GND	Ground
24	AC3	TMS	JTAG test mode select; internally pulled up with 10KΩ resistor
26	AA1	TDI	JTAG test data in; internally pulled up with 10KΩ resistor
28	AA2	TDO	JTAG test data out
30	K01	U0DSR	UART0 Data Set Ready.
32	T03	U0CTS	UART0 Clear To Send.
34	P04	U0TX	UART0 Serial Data Out.
36	T01	U0RX	UART0 Serial Data In.
38	J03	U1TX	UART1 Serial Data Out.
40	J02	U1RX	UART1 Serial Data In.
42	Y17	SYSERR	Set to 1 when a Machine Check is generated.
44	W22	IRQ0	Interrupt request 0. To access this function,software must toggle a DCR bit.
46	W23	IRQ1	Interrupt request 1. To access this function,software must toggle a DCR bit.
48	V21	IRQ2	Interrupt request 2. To access this function,software must toggle a DCR bit.
50	V22	IRQ3	Interrupt request 3. To access this function,software must toggle a DCR bit.
52	T22	IRQ4	Interrupt request 4. To access this function,software must toggle a DCR bit.
54	R20	IRQ5	Interrupt request 5. To access this function,software must toggle a DCR bit.
56	T23	IRQ6	Interrupt request 6. To access this function,software must toggle a DCR bit.
58		PCIREFCLK	PCI reference clock output synchronous with SycClk pin (ball AB18).
60	D22	PCIAD15	PCI Address/Data Bus.Multiplexed address and data bus.
62	D21	PCIAD14	PCI Address/Data Bus.Multiplexed address and data bus.
64	C23	PCIAD13	PCI Address/Data Bus.Multiplexed address and data bus.
66	C20	PCIAD12	PCI Address/Data Bus.Multiplexed address and data bus.
68	B20	PCIAD11	PCI Address/Data Bus.Multiplexed address and data bus.
70	A20	PCIAD10	PCI Address/Data Bus.Multiplexed address and data bus.
72	C19	PCIAD9	PCI Address/Data Bus.Multiplexed address and data bus.
74	D18	PCIAD8	PCI Address/Data Bus.Multiplexed address and data bus.
76	A19	PCIAD7	PCI Address/Data Bus.Multiplexed address and data bus.
78	C18	PCIAD6	PCI Address/Data Bus.Multiplexed address and data bus.
80	D17	PCIAD5	PCI Address/Data Bus.Multiplexed address and data bus.
82	B18	PCIAD4	PCI Address/Data Bus.Multiplexed address and data bus.
84	D16	PCIAD3	PCI Address/Data Bus.Multiplexed address and data bus.
86	B17	PCIAD2	PCI Address/Data Bus.Multiplexed address and data bus.
88	C16	PCIAD1	PCI Address/Data Bus.Multiplexed address and data bus.
90	B16	PCIAD0	PCI Address/Data Bus.Multiplexed address and data bus.
92	N20	PCIBE#3	PCI bus command and byte enable 3.
94	L20	PCIBE#2	PCI bus command and byte enable 2.
96	D19	PCIBE#1	PCI bus command and byte enable 1.
98	A18	PCIBE#0	PCI bus command and byte enable 0.
100	J20	PCISERR	PCISERR is used for reporting address parity errors or catastrophic failures detected by a PCI target.



<b>Pin</b>	<b>uP pin</b>	<b>Name</b>	<b>Description (102 to 200 - even )</b>
102	H20	PCIIRDY#	PCIIRDY# indicates that the PCI initiator is ready to transfer data.
104	G20	PCIRESET#	PCI specific reset.
106	F20	PCIREQ#1	Bus request from external master.
108	E20	PCIREQ#0	Bus request from external master.
110	J21	PCIPARITY	PCI parity.Parity is even across PCIAD00:31 and PCIBE3:0.
112	H21	PCIDEVSEL#	PCI target asserts PCIDEVSEL# when it has decoded an address and command encoding and claims the transaction.
114	G21	PCITRDY#	Assertion of PCITRDY# indicates that the PCI target is ready to transfer data.
116	F21	PCIGNT#2	Grant signal to external master requesting the bus
118	B21	PCICLK	PCIClk is used as the input asynchronous PCI clock when in asynch mode.
120	F02	RXD13	Ethernet interface 1: receive data
122	G03	RXD12	Ethernet interface 1: receive data
124	H03	RXD11	Ethernet interface 1: receive data
126	R01	RXD10	Ethernet interface 1: receive data
128	E02	RX1CLK	Ethernet interface 1: receive medium clock
130	D06	RX1DV	Ethernet interface 1: receive data valid
132	C01	RX1ERR	Ethernet interface 1: receive error
134	B05	PHY0CrS1	Carrier Sense signal from the PHY.
136	C05	PHY0Col1	Collision signal from the PHY.
138	D15	WE#	Peripheral write enable.
140	F03	WBE0#	These pin act as byte-enable
142	E01	WBE1#	These pin act as byte-enable
144	D02	PWR	Read/Write signal of Peripheral Bus
146	F04	POE#	Output Enable signal of Peripheral Bus
148		CSS	Chip Select selector input; CSS=L ⇒ PCS#0 at pin 150; CSS=H ⇒ PCS#1
150		PCS#0/PCS#1	Chip Select 0 output/ Chip Select 1 output (see pin 148 signal CSS)
152	E03	PCS#2	Chip Select 2
154	D03	PCS#3	Chip Select 3
156	D05	PCS#4	Chip Select 4
158	C04	PCLK	Peripheral clock to be used by peripheral slaves.
160	B03	PRDY	Ready to transfer data.
162	A09	PBLAST#	Used to indicate the last transfer of a memory access. To access this function,softwaremust toggle a DCR bit.
164	AB4	IIC SCL	I <sup>2</sup> C bus clock output; pulled up with 10KΩ resistor
166	Y01	IIC SDA	I <sup>2</sup> C bus data output; pulled up with 10KΩ resistor
168	A03	EXTRST#	External Reset
170	D01	D0 (LSB)	Least Significant Bit of the Data line for peripheral bus
172	F01	D1	Data line for peripheral bus
174	H04	D2	Data line for peripheral bus
176	G04	D3	Data line for peripheral bus
178	G02	D4	Data line for peripheral bus
180	J04	D5	Data line for peripheral bus
182	H01	D6	Data line for peripheral bus
184	K03	D7	Data line for peripheral bus
186	K02	D8	Data line for peripheral bus
188	L03	D9	Data line for peripheral bus
190	L02	D10	Data line for peripheral bus
192	M03	D11	Data line for peripheral bus
194	M02	D12	Data line for peripheral bus
196	P01	D13	Data line for peripheral bus
198	N04	D14	Data line for peripheral bus
200	P02	D15 (MSB)	Most Significant Bit of the Data line for peripheral bus

**Tab. 1 - SO DIMM Pinout connections**



## 6 - Pin Description and Off-Board Settings

User normally plugs PPChameleon boards over an host PCB where he designed its own interfaces and electronics working in combination. Some cautions must be used in order to get the maximum performance from PPChameleon board.

Furthermore, some settings are mandatory on the host board to get PPChameleon properly working. They are also summarized at the end of the chapter.

### 6.1.1 Power (1V8, 3V3 and GND) [J1 – pins 1-22]

Power consumption of the board is less than 3.0 Watt (@266 MHz clock) almost equally shared among 3.3V and 1.8V. Power is fed directly from host board. It means that user should be sure to provide at least this amount of current. Tolerances in power supply should not exceed +/- 5%. Refer to chapter 7 - for details related to power supply.

### 6.1.2 MRST# [J1 – pin 35]

This pin is a pulled up open- drain type [9]. Also reset circuitry on board is connected in an open drain mode. External circuitry must be of the same type as well. See [2] for details and examples.

### 6.1.3 IICSDA, IICSCL [J1 – pin 166/164]

If user wants to use these signals, should be aware that they are internally pulled-up through a 10KOhm resistor to 3.3V. No resistor is connected serially between the pin 166-164 of the SO-DIMM connector and the I2C pins of the processor.

This configuration is aiming a simple “standard-mode I2C”. Stronger pull-ups can be (often must be) therefore added on the host board in order to comply with higher bus speeds and/or bus capacitance charge.

### 6.1.4 OUT0, OUT1, OUT2, OUT3 [J1 – pin 23/25/27/29]

These four outputs are factory settings.

OUT0 provides a LVTTTL 25 MHz clock (+/- 100 ppm, 50% duty cycle) in order to feed second external PHY device. This to save an oscillator/quartz. OUT1, 2 and 3 are a selection of the led signals output by the Ethernet transceiver (STE100P) on-board (see also reference [8]). The OUT1, OUT2 and OUT3 signals are connected as shown in Tab. 2.

PPChameleon pin	STE100P pin	Description (for more details please see STE100P datasheet)
OUT1	ledl (pin 36)	LED display for Link Status. Blinks when there is TX or RX activity. This pin will be driven on continually when a good Link test is detected.
OUT2	ledtr (pin 37)	LED display for Tx/Rx Activity status. This pin will be driven on at a 10 Hz blinking frequency when either effective receiving or transmitting is detected.
OUT3	ledc (pin 35)	LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on at a 20 Hz blinking frequency when a collision status is detected in the half duplex configuration.



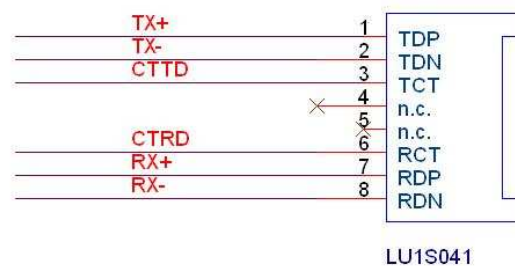
**Tab. 2 OUTx connections**

For further details, see manufacturer product documentation [8].

### 6.1.5 Tx+, Tx-, Rx+,Rx-, CTRR, CTRD [J1 – pin 189/191/193/195/197/199]

These pin are to be fed to magnetics and RJ45 with a certain care. Suggested magnetics are F0059 from InNet [5], and LU1S041 from Bothhand [4].

A possible design solution for Bothhand LU1S041 is depicted in Fig. 2.



**Fig. 2 - Connecting To Magnetics and RJ45**

### 6.1.6 CSS [J1 – pin 148]

CSS (Chip Select Selector) is pulled up with a 22K $\Omega$  resistor. This pin pulled low enables PCS#0 to be output at pin 150 ( see 6.1.7 ). At the same time PCS#1 is redirected as a Chip Select on internal NOR Flash.

On the other hand when CSS is tied up (as during regular operations) PCS#0 is redirected as a Chip Select on internal NOR Flash and PCS#1 is output on pin 150.

This features allows to debug code in the external SRAM during start-up, as disposed in the PPChameleon Evaluation Board. Also, it is possible to bootstrap from an external NOR Flash.

### 6.1.7 PCS#0-1 [J1 – pin 150]

Either PCS#0 or PCS#1 can be output on this pin. See 6.1.6 for details.

### 6.1.8 Summary of the bootstrapping options

Bootstrapping options are set either via embedded code [default] or via EEPROM. For more details please see [9], chapter 9.



## 7 - Power

Powering the module is a delicate operation. Since power must be provided from host board, users should be aware of the ranges power supply can assume.

In Tab. 3 are summarized nominal current consumptions at 3.3V and 1.8V.

Device	Type	3.3V	1.8V
CPU	I/O	70 mA	
CPU	Core		520 mA
CPU	PLL		17 mA
SDRAM	2 x K4S281632B (burst mode)	360 mA	
NOR Flash	M29W320 (writing)	20 mA	
NAND Flash	K9F5608 (writing)	20 mA	
Watchdog/Reset		≈ 0 mA	
Ethernet	STE100P	100 mA	
CPLD	LC4032	11 mA	
TOTAL		581 mA	537 mA
		≈ 1.9 W	≈ 1.0 W

**Tab. 3- Summary of the budgetary power consumption**

In Tab. 4 are summarized limits for power supply values.

	MIN	MAX
I/O power supply (3.3V)	3.15V	3.45
PLL and Core power supply (1.8V)	1.73	1.95

**Tab. 4 - Power supply ranges**



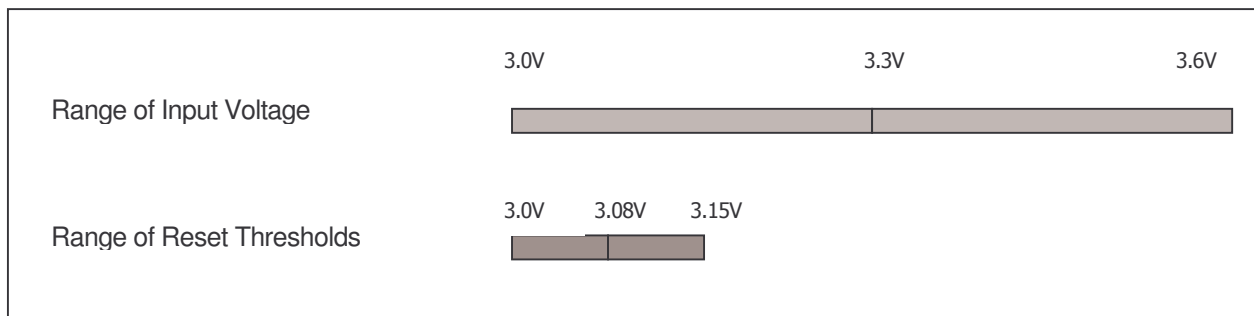
## 8 - Reset

In order to guarantee that microprocessor is monitored accurately, we should consider possible range of its supply, that are summarized below:

- 1.8V (min. 1.65V – max. 1.95V)
- 3.3V (min. 3.0V – max. 3.6V)

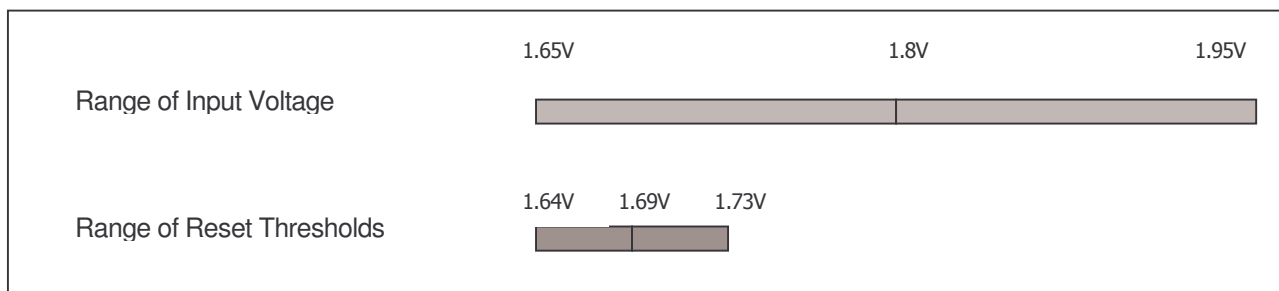
Due to the fact that power supply regulation is provided from external circuitry, it is mandatory to monitor accurately both voltages.

As far as 3.3V is concerned, a reset threshold at 3.08V with a maximum, possible temperature variation of  $\pm 2.5\%$  in the range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  has been adopted. In practice reset threshold has a variation from 3.00V to 3.15V all over the extended temperature range.



**Fig. 3 – Graphical representation of reset thresholds for 3.3V [ $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ]**

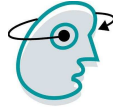
Same considerations hold for 1.8V supply as in Fig. 4.



**Fig. 4 - Graphical representation of reset thresholds for 1.8V [ $0^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ ]**

This combined values – although in a extended temperature range – limit in practice the range of possible power supply voltages in the range 3.15 to 3.6V for I/O supply voltage, and 1.73V to 1.95V for Core voltage.

Limitation to 3.15V-3.45V and 1.73V-1.95V is due to the other component retrictions. See Chapter 7 - for that.



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## 9 - History

Rev.	Date	Hw Rev.	EVB Hw Rev.	Details
0.9	May 03	CS111303	CS121703	Preliminary specs
0.91	June 03	CS111303B	CS121703B	Modified pin-out, modified functionality for external CS
1.0.0	Aug 03	CS111303B	CS121703C	Further modifications
1.1.0	Oct 03	CS111303C	CS121703C	Released with PELK 1.1.0
1.2.0	Feb 04	CS111303C	CS121703C	Released with PELK 1.2.0
1.3.0	May 04	CS111303C	CS121703C	Released with PELK 1.3.0 Fixed section about OUTx signals

## 10 - Support

To contact technical support, please send an e-mail to address [support-ppchameleon@dave-tech.it](mailto:support-ppchameleon@dave-tech.it).

## 11 - References

- [1] DAVE PPChameleon Embedded Linux Kit – Software Manual
- [2] DAVE PPChameleon Evaluation Board EVB User Manual
- [3] JEDEC Standard No. 21-C, module 4.20.6: ([www.jedec.org](http://www.jedec.org))
- [4] JEDEC Standard No. MO224-A: ([www.jedec.org](http://www.jedec.org))
- [5] AMP site ([www.amp.com](http://www.amp.com))
- [6] DELPHI site (<http://www.delphi.com/connect/IndustryStandards/>)
- [7] JAE site (<http://www.jae-connector.com/en/index.cfm>)
- [8] STM, STE100P data sheet
- [9] PowerPC 405EP Embedded Processor Users's Manual – IBM