

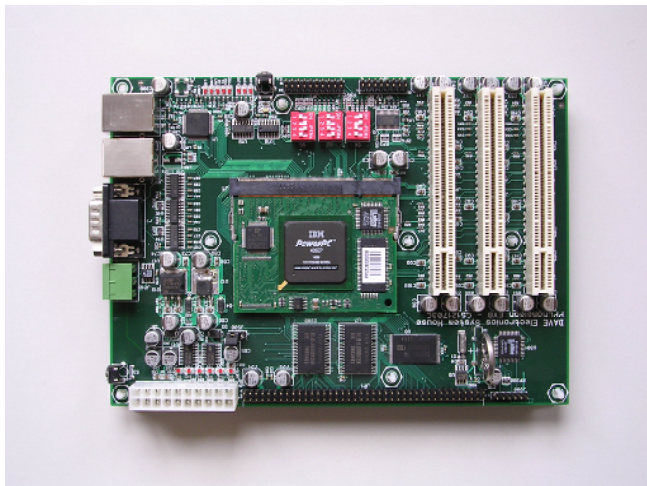
# "PPCHAMELEON"<sup>®</sup>

PowerPC 405EP

Evaluation Board & Development Kit



- CPU module based on PowerPC 405EP
- PCI host bus + Expansion Bus fully available
- NAND Flash on-board (option) + JFFS2 filing system
- Ready for Linux 2.4.20 + native component drivers
- Evaluation Board available with exhaustive development kit
- DDR 200 SODIMM compact form factor, inexpensive connector
- Development Kit available in GNU environment
- ITE & ISM approvals
- Ready For IBM Technology



**PPCHAMELEON Evaluation Board & Development Kit** supports ready-to-use CPU module based on IBM PowerPC 405EP **PPCHAMELEON**. All *native* buses and interfaces of the microprocessor are on the board or routed to separate connectors. Therefore users may perform full on-boards tests or think flexible design integrations. A complete software suite named PELK (**P**owerPC **E**mbedded **L**inux **K**it) is provided with **PPCHAMELEON** Evaluation Board. This software not only allows a straightforward use of GNU toolchain, but is also continuously up to date and maintained with new peripherals, applications and drivers. **PPCHAMELEON**

Evaluation Board is a flexible and complete system where users can test their own applications or add their own expansion boards:

- ATX PSU
- SODIMM connector for PPChameleon Module
- NAND + CPLD bus adaptation
- SRAM for bootcode debugging
- PCI clocking circuitry
- JTAG and TRACE interfaces
- Bootstrapping circuitry (FLASH or SRAM)
- 3 PCI slots
- Expansion Bus connector
- RTC with back-up battery
- 2<sup>nd</sup> PHY 10/100 + 2 RJ45 including magnetics
- RS485 + full RS232



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### **CPU Module**

|        |   |
|--------|---|
| PPC-BA | PPC Module @133MHz, 4MB Flash, 32MB SDRAM             |
| PPC-ME | PPC Module @266MHz, 4MB Flash, 32MB SDRAM, 32MB NAND  |
| PPC-HI | PPC Module @333MHz, 4MB Flash, 32MB SDRAM, 128MB NAND |

### **Memory**

|            |                 |
|------------|-----------------|
| Flash NAND | 32 Mbytes       |
| SRAM       | 512K x 16 Bytes |

### **Others**

|      |   |
|------|---|
| CPLD | for various NAND driving                                |
| RTC  | via I2C bus + backup lithium battery                    |
| PCI  | PCI skew-controlled clock distribution, spread spectrum |

### **Interfaces**

|                  |   |
|------------------|---|
| Ethernet         | nr.2 RJ45   |
| UART             | nr.1 full (5+3)   |
| RS485            | nr.1  |
| I <sup>2</sup> C | Master/slave/multimaster 400kHz                                   |
| External Bus     | 16-bit / 29 Address Bits -5 direct Chip Select; bus speed < 66MHz |
| PCI              | nr.3 slots 5V host (version 2.2), arbiter supporting 3 devices    |
| I/O Controller   | yes, number tbd   |

### **Debug Interfaces**

|      |  |
|------|--|
| CPU  | JTAG IEEE 1149.1 Test Access Port              |
| CPU  | IBM TRACE                                      |
| CPLD | JTAG IEEE 1149.1 Test Access Port (precharged) |

### **Mechanical**

|             |  |
|-------------|--|
| Connectors  | 200 pin DDR SO-DIMM (JEDEC MO-224) <i>double height</i> format |
| Physical    | 140 (w) x 195 (l) x 31 (h) mm <sup>3</sup>                     |
| PCB         | 6 layers   |
| Material    | FR4  |
| Technology  | SMT  |
| Temperature | 0 ÷ 70 °C operational temperature                              |

### **PSU**

|           |                 |
|-----------|-----------------|
| Generator | ATX standard    |
| Connector | 20 pins Minifit |
| Start     | Pushbutton      |

### **Agency approvals**

|         |   |
|---------|---|
| CE Mark | ITE & ISM<br>EN 55022, EN 55011, EN 55024 |
|---------|---|

Informations and sales

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